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Diogo Carlos Alcobia Ribeiro

Sistema de Medida Analógico-Digital para Software-Defined Radios

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Analog-Digital Measurement System for Software-Defined Radios

Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia de Electrónica e Telecomunicações. Realizada sob a orientação científica do Professor Doutor Nuno Miguel Gonçalves Borges de Carvalho, Professor do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro, e colaboração do Mestre Pedro Miguel Duarte Cruz.

Aos meus pais.

o júri / the jury

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Palavras-chave SDR, Software Defined Radio, VNA, Vector Network Analyzer, ADC, DAC

Resumo

Esta dissertação insere-se na área de metrologia de rádio-frequência, procurando colmatar a actual lacuna de instrumentos capazes de caracterizar rápida e eficazmente um componente analógico-digital, tal como uma ADC ou DAC. Estes componentes são elementos chave da concepção de arquitecturas Software-Defined Radio (SDR).

O conceito de SDR define um rádio que seja totalmente adaptável por software, através da transição de blocos do domínio analógico para o domínio digital. Assim sendo, a adopção destas arquitecturas rádio irá ser cada vez mais utilizada de forma a responder à crescente necessidade de receber diversos tipos de comunicação num único terminal.

Neste trabalho propõem-se a implementação de um instrumento que caracterize componentes analógico-digitais da mesma forma que o tradicional e popular Vector Network Analyzer (VNA) faz para componentes analógicos. Procura-se fornecer a um projectista de rádio, uma ferramenta que permita prever o desempenho de um componente analógico-digital do ponto de vista de rádio, de forma a facilitar o projecto de novos e mais complexos sistemas SDR.

A implementação proposta pretende caracterizar componentes na banda de frequências dos 40 aos 1000 MHz. Diversos ensaios foram realizados de forma a mostrar à comunidade científica a mais-valia deste instrumento.

Keywords SDR, Software Defined Radio, VNA, Vector Network Analyzer, ADC, DAC

Abstract

This thesis is inserted into the Radio-Frequency metrology, it pursuits to fulfil the current gap of instrumentation able to characterize analog-digital components, as ADC or DAC's, in a quickly and effective form. These analog-digital components are the key to the conception of Software-Defined Radio (SDR) architectures.

The SDR concept defines a radio system totally implemented by means of software, where the of most the components operate in digital domain. Therefore, these architectures are becoming more and more used due to the growing need of receiving different kinds of communications in only one terminal.

This paper tries to set up an instrument capable of characterize mixed-domain components as the tradicional and popular VNA can do with analog components. It is tried to built a new brand tool that can give to the radio designer, an easy form to create other SDR complex projects.

The proposed instrument pretends to characterize components from 40 to 1000 MHz bandwidth. Several tests were made in order to show its added value to the scientific community.

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Acronyms

1G First Generation.

2G Second Generation.

3G Third Generation.

4G Fourth Generation.

ADC Analog-to-Digital Converter.

ADS Advanced Design System.

AM Amplitude Modulation.

AMPS Advanced Mobile Phone System.

ASCII American Standard Code for Information Interchange.

AWG Arbitrary Waveform Generator.

BER Bit Error Rate.

BPF Band-Pass Filter.

BPSK Binary Phase-Shift Keying.

CMOS Complementary Metal–Oxide–Semiconductor.

CR Cognitive Radio.

CW Continuous Wave.

DAC Digital-to-Analog Converter.

DC Direct Current.

DCM Digital Clock Manager.

DCOM Distributed Component Object Model.

DIP Dual In-line Package.

DSP Digital Signal Processor.

DUT Device Under Test.

EDGE Enhanced Data rates for GSM Evolution.

ENOB Effective Number Of Bits.

EVM Error Vector Magnitude.

FFT Fast Fourier Transform.

FIFO First In, First Out.

FM Frequency Modulation.

FPGA Field Programmable Gate Array.

FSK Frequency-Shift Keying.

GPIB General Purpose Interface Bus.

GSM Global System for Mobile Communications.

GSPS Giga-Samples Per Second.

GUI Graphical User Interface.

HP Hewlett-Packard.

I/O Input/Output.

I/Q In Phase/Quadrature.

IC Integrated Circuit.

ICNIA Integrated Communications Navigation and Identification Avionics.

IF Intermediate Frequency.

IFT Inverse Fourier Transform.

IIP3 Input Third-order Intercept Point.

IM3 Third-Order Intermodulation.

IMD Intermodulation Distortion.

IMR Intermodulation Ratio.

IP Internet Protocol.

IP_3 Third-order Intercept Point.

IS-95 Interim Standard 95.

ISM Industrial, Scientific and Medical.

IT Instituto de Telecomunicações.

IVI Interchangeable Virtual Instrument.

LA Logic Analyzer.

LAN Local Area Network.

LDO Low-Dropout Regulator.

LNA Low Noise Amplifier.

LO Local Oscillator.

LPF Low-Pass Filter.

LSNA Large Signal Network Analyzer.

LTE 3GPP Long Term Evolution.

LVDS Low-Voltage Differential Signalling.

MDO Mixed Domain Oscilloscope.

MSO Mixed Signal Oscilloscope.

MSPS Mega-Samples Per Second.

MTA Microwave Transition Analyzer.

NF Noise Figure.

OFDM Orthogonal Frequency-Division Multiplexing.

OIP3 Output Third-order Intercept Point.

OSM Open, Short, Match.

P1dB 1 dB Compression Point.

PAPR Peak-to-Average Power Ratio.

PC Personal Computer.

PCB Printed Circuit Board.

PM Phase Modulation.

QAM Quadrature Amplitude Modulation.

QoS Quality of Service.

QPSK Quadrature Phase-Shift Keying.

R&S Rohde & Schwarz.

RF Radio Frequency.

RL Return Loss.

SCPI Standard Commands for Programmable Instruments.

SDR Software Defined Radio.

SFDR Spurious-Free Dynamic Range.

SINAD Signal-to-Noise And Distortion ratio.

SMA Sub-Miniature version A.

SMD Surface Mount Device.

SNA Scalar Network Analyzer.

SOIC Small-Outline Integrated Circuit.

SOL Short, Open, Load.

SOLT Short, Open, Load, Thru.

SOT Small-Outline Transistor.

T&M Test and Measurement.

TDT Televisão Digital Terrestre.

TI Texas Instruments.

TQFP Thin Quad Flat Pack.

TRL Trough, Reflect, Line.

TTL Transistor–Transistor Logic.

UHF Ultra High Frequency.

UMTS Universal Mobile Telecommunications System.

USB Universal Serial Bus.

VHDL VHSIC Hardware Description Language.

VISA Virtual Instrument Software Architecture.

VNA Vector Network Analyzer.

VSA Vector Signal Analyzer.

Wi-Fi Wireless Fidelity.

WiMAX Worldwide Interoperability for Microwave Access.

Chapter 1

Introduction

Wireless communications have been having a great development since its inception. From the appearing of analog modulated transmissions, the wireless communications have been growing in popularity and number of users. Firstly with the AM broadcast radio and later with FM broadcast radio. FM transmissions became to emerge in the 20th decade and even nowadays are still used for broadcasting and for emergency communications.

Lately, near the 80's, the first cell phone appeared. Developed by Bell Labs, the analog system was named Advanced Mobile Phone System (AMPS). Due to its popularity, an enormous number of people became to use it and in spite of being a great advance to that period, it's capacity was unable to accommodate all the clients. The AMPS was recognized as the First Generation (1G) communication.

In the 1990, the migration to digital systems came to solve the previous issue. Europe adopted GSM and USA, the IS-95. With the Second Generation (2G) installed, it was reached a massif use of mobile phones, reaching a penetration tax above one hundred per cent in global population. This generation were built mainly for voice services and slow data transmission although the appearing of web popularity demands for higher data transfer. So an evolution of the 2G rises, to build a bridge between this and the next generation, the GSM and EDGE with a transmission rates that variate from 56 Kbits/seg to 115 Kbits/seg came to light. However the even higher demands for data streams motivate the appearing of the Third Generation (3G) networks.

3G era was very important because it brought a big step in transmission data rates. With the UMTS in Europe and CDMA2000 in USA, 3G could reach up to 45 Mbits/seg (theoretically).

The Fourth Generation (4G) is being developed and implemented right now, it is excepted to provide comprehensive and secure all-IP based mobile broadband. For that, an efficient Quality of Service (QoS) had been developed. LTE "pre-4G technology" offers a transmission rate of 100 Mbit/seg (for downloads) and 50 Mbit/seg (for uploads).

In the last years other new communication services appeared. For example, the Wi-Fi brings wireless internet and multimedia services to computers and other equipments. Currently, it reaches an enormous popularity and it already has some sort of evolution, the WiMAX.

For many applications which not demand for high transmission rates, but instead need low power consumption, other communications types based on different protocols, had been developed, such as the Bluetooth and the ZigBee.

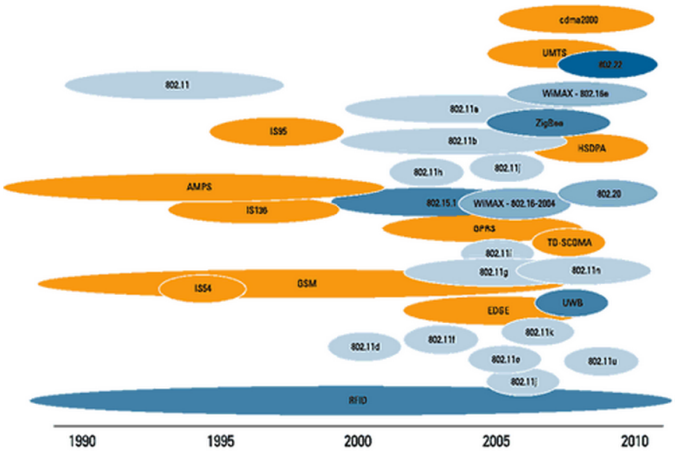


Figure 1.1: Wireless Protocol Increase, from [1]

As can be seen, through the time, many communication types came to solve our growing needs. Each one needs a different hardware implementation. SDR, due to its characteristics, is capable of solve this issue.

1.1 Motivation

The Software Defined Radio (SDR) in its definition allows for a full reconfigurable transceiver. As the receiver or emitter blocks are totally implemented in software they could change in order to adapt themself to other parameters. So the SDR could be used to receive different types of communication at different times, or even at the same time.

This huge advantage over the traditional receivers or emitters is the key point, that makes the need for SDRs more and more high. With the enormous number of different kinds of communications, with a vast set of modulations and based in several different protocols, a radio which could communicate in all this scenarios is an enormous advantage.

However, the tools available in nowadays RF labs aren't capable to evaluate mixed-domain components in an easy and direct way. Mixed-Domain components, such as ADCs or DACs, are the basis of an SDR. For this reason a new SDR project is much more difficult, that it could be.

Following the M.Sc. Pedro Cruz work [8], the propose of this work is to build an instrument that can measure the frequency response of a mixed-domain component or an entire SDR in an easy and complete way.

1.2 Document Overview

This dissertation is organized into six chapters and three appendices. Here are the outline of these parts:

The **Chapter 1** introduces the dissertation.

In **Chapter 2** is presented an introduction to the SDR concept and to the architectures that could be adopted to implement it.

In **Chapter 3** an overview to part of the actual instrumentation portfolio is shown. Some general purpose instruments and the most common RF instruments are presented and its functions succinctly described. The Mixed-Domain instrument proposed is also presented.

The **Chapter 4** describes the implementation steps to accomplish the desired performance on each block of the proposed instrument design. The implementation steps are split into 2 stages, the analog and the digital stage. Further, all the instruments used to complement the proposed one are referred and the communication between them and the control unit are described.

The **Chapter 5** explains the entire measurement procedure. From the method used to perform the frequency sweep measurement, through the details of the acquisition method used, until the calibration procedure implemented (in this topic a deep analysis of the actual used calibration processes are also presented). Finally, it is presented the graphical user interface created to take measurements.

In **Chapter 6** several results taken from the implemented instrument are shown and compared with the results obtained in a commercial VNA.

The **Chapter 7** presents the final conclusion and some ideas to future work.

The **Appendice A** presents and describes a method based on existing literature, to characterize frequency translating devices with an oscilloscope.

In **Appendice B** all the GUI functionalities are described in order to produce a manual to the user.

In the **Appendice C** are presented all the PCBs and schematics of the implemented hardware.

Chapter 2

Software Defined Radio

2.1 Introducing the Concept

The concept of Software Defined Radio (SDR) was introduced in the early 1990s by Joseph Mitola. His work described SDR as a fully adaptable radio, a radio that can receive multiple signals with different modulations with the same hardware. This concept attempts to do the signal processing as much as possible in the digital domain.

To achieve this, in the ideal SDR the Analog-to-Digital Converter (ADC) and the Digital-to-Analog Converter (DAC) will be as close as possible to the antenna, as shown in figure 2.1. In there the antenna is preceded by an circulator, in this component all the signals that travels into one port are transmitted to the next port considering the rotational way displayed. Therefore, even with only one antenna the transmitter and receiver chains are independent.

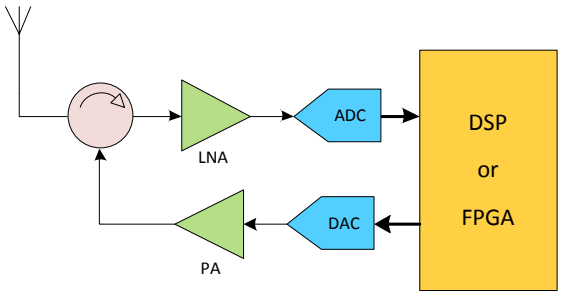


Figure 2.1: Ideal SDR architecture

With this configuration, in the receiving process the ADC will digitize every signals that appears on the antenna and then a digital processing unit will compute every necessary steps in order to recover the final wanted signal. This includes amplification, filtering, down-conversion and demodulation. As these steps are made in digital domain, this receiver can switch from multiple signals with different frequencies, power, modulations, and other signal characteristics making it reconfigurable and adaptable to a certain need at a certain time.

As said before, the term SDR had been introduced to the world by Mr. Mitola, although some other projects, previous to Mitola's work, already use an SDR approach to communicate. At least the ICNIA U.S. military program[9], in the 1970's, as already start to explore the SDR concept.

After Mitola's publication many other research projects focused their efforts on this mater.

In the final 1990's commercial radios using SDR approach started to be sold, with principal incidence on cellular infrastructures.

2.2 Cognitive Radio

With the evolution of SDR concept a new keyword appears: *Cognitive Radio (CR)*. It defines not only a fully adaptable radio, but also a radio that can evaluate its surrounding spectra and decide which is the best way to transmit and/or receive information. Once again Mr. Mitola was the author who defined this term. By his words:

> *"Cognitive radio is a goal-driven framework in which the radio autonomously observes the radio environment, infers context, assesses alternatives, generates plans, supervises multimedia services, and learns from its mistakes. This observe-think-act cycle is radically different from today's handsets that either blast out on the frequency set by the user, or blindly take instructions from the network. Cognitive radio technology thus empowers radios to observe more flexible radio etiquettes than was possible in the past."* [10]

2.3 Front End Receiver Architectures

In the ideal SDR architecture, to digitize all the signals in the full spectrum, will be necessary an ADC with infinite sampling frequency. Nowadays, it still is a far reality, therefore other architectures to the front end receiver are possible to be implemented. These architectures can be characterized by the frequency of the signal digitized in the ADC and by the topology of the receiver chain. In this section several architectures are succinctly reviewed, organized by the position of the ADC on the receiver chain.

2.3.1 Baseband Digitalization

The most commonly used architecture in analog radios is the well known super-heterodyne receiver, his counterpart on SDR front end has the ADC positioned at the baseband stage, figure 2.2. As the Baseband signal is a low frequency signal the ADC requirements are minimized, even with a very high radio frequency, and the conversion from Intermediate Frequency (IF) is often done using an in-phase quadrature (I/Q) demodulator, as shown. However several problems are inherent to this architecture, the image frequency, his narrowband characteristic and the high number of components used. These problems make this configuration not so suitable to use on SDR receivers.

To solve the image frequency problem, like on conventional receivers, an homodyne topology could be used instead. It is also named as zero-IF. This architecture can be done taking out the IF stage from the super-heterodyne receiver and setting the LO1 frequency to the same frequency of the Radio Frequency (RF) signal, resulting in a direct conversion to baseband. With this configuration additional advantages are achieved, like the minimization of the number of components used and the maximization of the bandwidth. Although, as on conventional receivers, another problems will appear. The direct conversion to baseband will dictate the need for a much better local oscillator and a DC offset could arise.

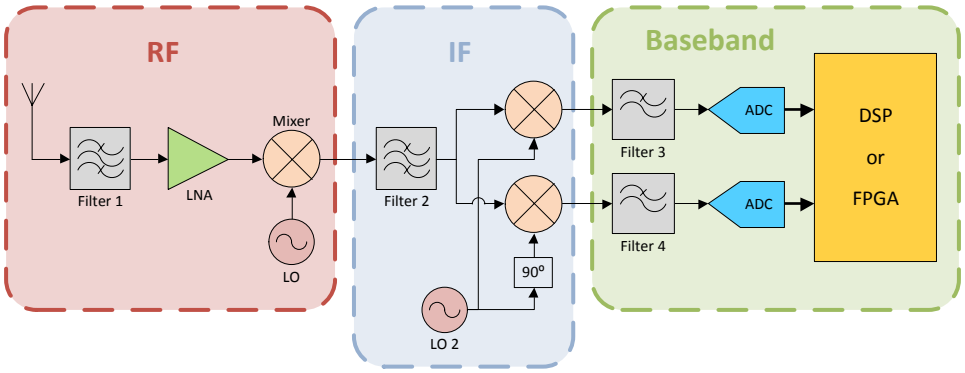


Figure 2.2: Baseband digitalization architecture

2.3.2 IF Digitalization

In order to reduce the number of components and at the same time avoid the homodyne issues, the receiver chain could be rearranged. Instead of convert the RF signal directly to baseband, it can be converted to an IF and then directly digitized by the ADC. This makes the design of the local oscillator less critic, although the problem of frequency image reappears which makes the complexity of the image reject filter to grow up again and can limit the receiver bandwidth if a low-IF was used.

However this architecture could be used with an high IF even with an ADC that doesn't have a sampling frequency as high as the IF. This is possible due to the sampling process and his characteristics that can be used to perform a bandpass sampling.

To correctly understand the bandpass sampling, the entire sampling process will be shortly explained before the return to the actual discussion.

Sampling Process

The sampling process at the sampling frequency f_S can be mathematically described as the multiplication of the original signal $x(t)$ by a periodic impulse train, $p(t)$, with period $T_S = \frac{1}{f_S}$, so:

$$x_S(t) = x(t)p(t) = \sum_{n=-\infty}^{+\infty} x(t)\delta(t - nT_S) \tag{2.1}$$

The equation 2.2 express the Fourier transformation of the resulted sampling signal $x_S(t)$. From this expression can be noticed that the spectrum of the resulting signal is a sequence of replicas of the original signal spectrum spaced by f_S.

$$X_S(f) = F_S \sum_{k=-\infty}^{+\infty} X(f - kF_S) \tag{2.2}$$

As the signals that need to be sampled are real signals, the resulted sampled spectrum can be split into Nyquist zones, spaced by $f_s/2$. In each one of these zones the spectrum will be the mirror image of the previous and the next Nyquist zone. Thus to avoid superposition of the original spectrum and consequently degradation of information, the original signal must be bandwidth limited to $f_s/2$. This limitation is wide known as Nyquist theorem.

The same effect that up converts an original baseband signal within the first Nyquist zone to every others zones will also down converts an signal at an higher Nyquist zone to every others zones, including the first one. Using this effect with the knowing of the limitations of the Nyquist theorem can be much useful to translate higher frequency signals directly to base-band.

From the result of the process, can be extracted that a signal at a frequency f_c within an odd Nyquist zone will lie at the first Nyquist zone as an inverted image of the original signal, and if the f_c frequency was within an even Nyquist zone, the signal lie at the first Nyquist zone as the non-inverted image of the original signal. This relation can be defined as expressed on the equation 2.3.

$$\text{If} \quad \text{fix}\left(\frac{f_C}{f_S/2}\right) \quad \text{is} \begin{cases} \text{even}, & f_{IF} = \text{rem}(f_C, f_S) \\ \text{odd}, & f_{IF} = f_S - \text{rem}(f_C, f_S) \end{cases} \tag{2.3}$$

On the figure 2.3 an example of how the sampling process will affect the sampled signal on the frequency domain is depicted.

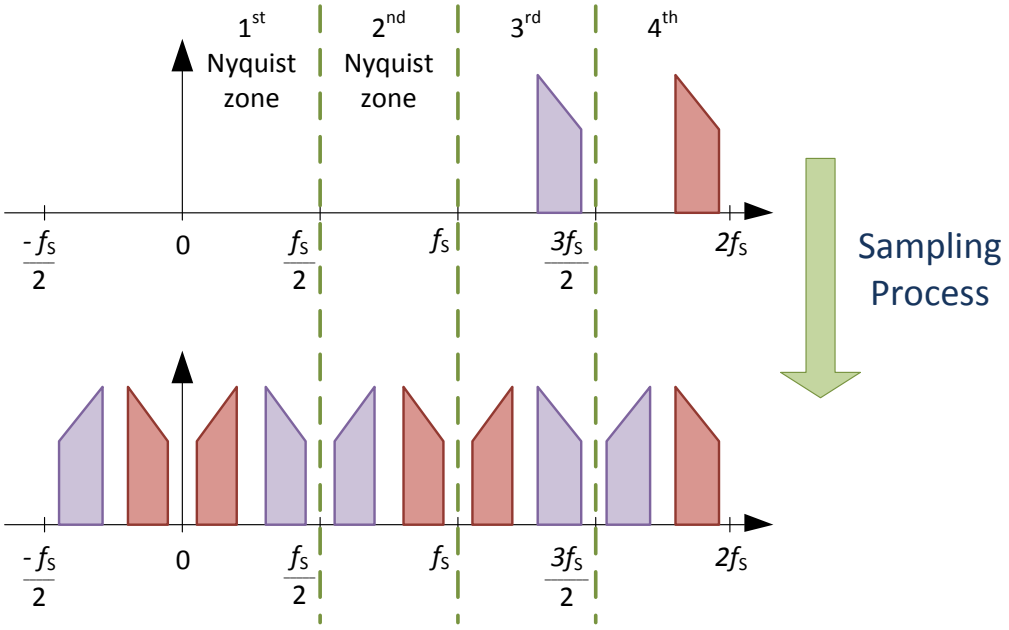


Figure 2.3: Sampling Process Description

As shown, if it is possible to accommodate all the spectrum replicas on the first Nyquist zone without superposition, the signal won't suffer from aliasing and won't be degraded, even if the entire bandwidth of the original signal was higher than $fs/2$. Although the sum of the several signal bands never can exceed $fs/2$.

Returning to our receiver chain, with the bandpass sampling process and the ability to put the ADC receiving an high IF, the architecture is constructed as depicted on figure 2.4. There, the Filter 2 is the anti-aliasing filter which has to ensure that after the digital conversion there is no superposition on the first Nyquist zone.

With this receiver chain topology, the digital operations increased and the number of analog components decreased. As a result, the overall reconfiguration of the receiver is improved."

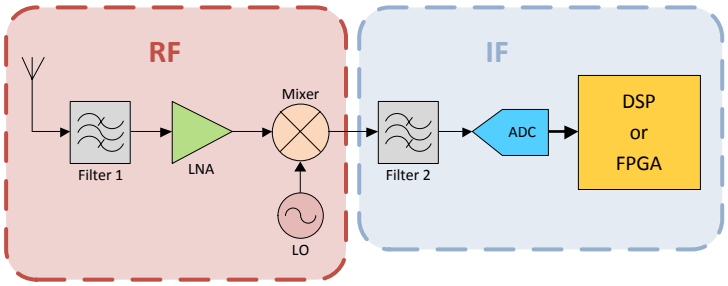


Figure 2.4: IF digitalization architecture

2.3.3 RF Digitalization

This architecture is the closest to the ideal one presented by Mr. Mitola. It takes, once again, use of the proprieties of the already mentioned bandpass sampling to directly down-convert the RF signal to base-band. The difference from the ideal architecture to this one is the presence of an anti-aliasing filter, represented by Filter 1 on figure 2.5. This filter has to exist due to the finite sampling frequency of the ADC and his complexity has a direct relationship with f_S, since the lower the f_S the higher has to be the complexity of the filter.

However the biggest limitation on this architecture was the analog bandwidth of the ADC's sampling and hold circuitry. As this circuit is not ideal, it will act as an low pass filter and so the ADC could not be capable of digitize directly the RF signal.

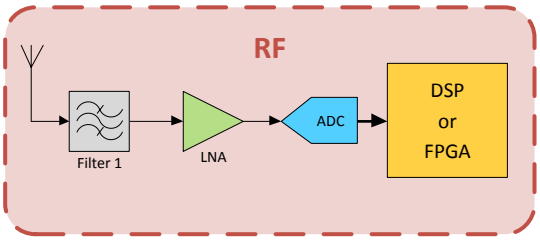


Figure 2.5: RF digitalization architecture

Chapter 3

Measurement Instrumentation

3.1 General Purpose

3.1.1 Oscilloscopes

The oscilloscope is the most immediate way to measure a signal that an engineer can have. It allows to watch the voltage waveform in time.

Older oscilloscopes used an all analog front-end. They controlled a cathode ray tube to display the input waveform voltage. Nowadays, oscilloscopes use a digital front-end similar to the RF Digitalization presented before, where an ADC directly digitize the voltage signal of interest. Typically oscilloscopes uses 8 Bit ADCs to reproduce the signal in detail. The use of this front-end was only possible due to the extreme increase in the ADCs sampling rate[1].

State of the art oscilloscopes have ADCs as fast as 100 Giga-Samples Per Second (GSPS) and a bandwidth as high as 33 GHz.

In common propose oscilloscopes, the connection between the port of the oscilloscope and the point of the circuit to be measured is made by a probe. This probe should be chosen to match the measurement needs as it can measure current, differential voltages, or single ended voltages. Voltage probes have high impedance to don't disturb the measured circuitry. However, it must have in mind that the impedance seen by the probe must be much lower than itself.

In high frequencies, another issue appears and the typically passive probes used on ordinary oscilloscopes have to be replaced by active probes. Because the probe's input high impedance associated with its input capacitance will behave as a low pass filter. In oscilloscopes used to RF purposes, 50 Ω inputs are used instead of high impedance inputs, this way the oscilloscope will act as a load to the measured circuit and it should be seen as a part of the circuit, the receptor.

Trigger controls are crucial to capture the wanted waveform in the right moment and to stabilize repetitive waveforms [11]. Trigger in oscilloscopes are simple events originated by one of its inputs (main ones or auxiliaries). Trigger events don't depend only on the level of the trigger source, they depend on the behaviour of the trigger source signal. Several trigger set ups could be configured in order to obtain the wanted waveform portion. Digital oscilloscopes allow the user to define the horizontal trigger position, i.e. by taking into memory the signal

[1]The referred oscilloscopes are known as Real-Time Oscilloscopes. On the other hand Equivalent-Time Oscilloscopes or just Sampling Oscilloscopes have low sampling rates but they could digitize signals with a frequency much higher than its sampling rate.

before the trigger event, they are able to display the waveform even before the trigger. The trigger holdoff is a parameter that defines the amount of time in which the oscilloscope won't trigger after a valid trigger event occur.

3.1.2 Logic Analyzers

The Logic Analyzer (LA) stay for a digital signal as the oscilloscope stay for an analog signal. The LA allows to watch a digital signal in time. One of the obvious difference between the two is the number of channels. While LAs have several channels, from 34 to hundreds of channels, an oscilloscope has only 2 or 4 channels [12], typically.

More than this, as the purpose of the LA is to acquire digital signals it only take the logic value of the signal. So, instead of digitize the voltage signal with an 8 or 10 Bits ADC, as the oscilloscope generally does, the LA simply compares the input signal to a user defined voltage threshold (V_{th}). Then if the signal is above V_{th} it is considered a Logic "1", if it is below, it is considered a Logic "0". This acquisition system is represented on figure 3.1.

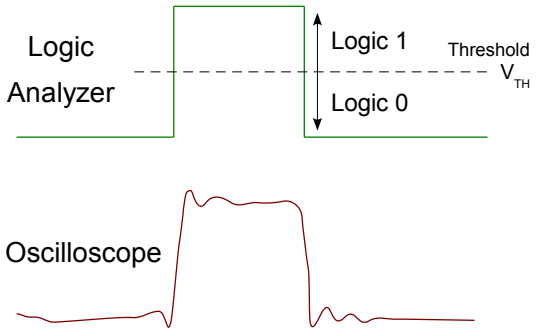


Figure 3.1: Logic Analyzer versus Oscilloscope waveforms

The LA is able to capture digital signals in many different logic families, such as CMOS, TTL, LVDS and many other. Beyond this, it is commonly possible to set an user value to the voltage threshold.

Furthermore, the Logic Analyzer is able to capture the signal with synchronous sampling, which in most case is the only way to acquire faithful results. Taking the example of an ADC, if it is needed to read its digital output, the signals must be acquired with the ADC output clock in order to has the correct information sampled by it.

Logic Analyzers also use probes to acquire the signal. The general purpose probes are "flying leads", with them it is possible to acquire signals at distinct points. Although, there are several other probes with specific end-connectors to attach it to an installed compatible connector.

Pattern Generator

Included in the LA instrument is usually a Pattern Generator. It could generate digital signals.

3.1.3 Mixed Signal Oscilloscopes

Recently, instrumentation industry present a new instrument that combines the ability to faithful reproduce analog signals of the oscilloscope with the ability to read multiple digital signals of the LA. This instrument is called Mixed Signal Oscilloscope (MSO).

Mainly it is an Oscilloscope with 2 or 4 ports to receive analog signals and in the same instrument there are also available several digital ports to receive the digital signals. It has the great advantage of being able to time correlate both signals.

However, the MSO digital front-end lacks the Synchronous Acquisition feature found on Logic Analyzers. Thus, MSOs use their own clock to sample the digital signal, as the oscilloscopes do to sample the input signal. As explained on [13] using asynchronous sampling to sample again a digital signal, the magnitude and phase information retrieved from the captured signal could be completely corrupted.

From the above perspective it will be better to use an Oscilloscope together with an LA to acquire correlated in time mixed-domain signals. In this scenario, there is for sure another problems such as triggering mismatches issues which could trouble the measurement, but if they are possible to avoid much better results are accomplished.

3.1.4 Mixed Domain Oscilloscope

In the last months the instrumentation industry launched another new instrument. They called it Mixed Domain Oscilloscope (MDO). It packs the MSO abilities and join them the ability to measure RF signals. This RF measure is done with an IF digitalization front-end, in the same way it is done in modern Spectrum Analyzers, that will be discussed later on the section 3.2.3.

More specifically it was Tektronix who presented to the world the MDO4000 Series[14]. Until now any other manufacturer has launched an equivalent instrument.

3.2 RF Instrumentation

In order to correctly characterize and test RF components, several instruments was developed with a specific measurement function. RF components are more changeling to measure due to its high frequency operation, which in old days doesn't allow the use of oscilloscopes and other general purpose instrumentation.

In this section a briefly description of main RF instrumentation are presented. Besides the instruments presented there are others to accomplish for different measures, as the:

- Noise Figure Meter – It is employed in the measure of a component Noise Figure (NF).
- Vector Signal Analyzer (VSA) – It is used to measure Error Vector Magnitude (EVM), Bit Error Rate (BER), etc.

3.2.1 Signal Generators

To test RF components or systems, an appropriate signal must be generated to feed the Device Under Test (DUT). The employed signal generator should be able to produce it. Usually, a Signal Generator provide the manipulation of the following proprieties:

- Frequency
- Power
- Analog Modulation
    1. Continuous Wave (CW)
    2. AM
    3. FM
    4. Phase Modulation (PM)[2]

The Vector Signal Generators are a subtype of Signal Generators. Which, besides the previous characteristics also allows the use of digital Modulations, such as as Quadrature Amplitude Modulation (QAM), Quadrature Phase-Shift Keying (QPSK), Binary Phase-Shift Keying (BPSK), Frequency-Shift Keying (FSK) and Orthogonal Frequency-Division Multiplexing (OFDM).

Besides the modulations types presented before some two-tone or N-tone signals could be generated also. If this is not enough it is possible to produce any type of signal using an Arbitrary Waveform Generator (AWG).

Arbitrary Waveform Generator

The AWG is a specific kind of signal generators. It has embedded a DAC so, it is able to reproduce a signal pre-generated by the user. This signal could be just a baseband signal, which is next up-converted, or if the DAC has enough speed, it could be directly the RF signal. The wanted signal could be generated directly on the instrument with some auxiliary tool or, it usually could be produced on other software as MATLAB®and then sent to the instrument.

State-of-the-art AWGs has 12 GSPS, 12 bits DACs and could manage to reach 24 GSPS using interleaving, with an analog bandwidth of 5 GHz.

3.2.2 Power Meters

The power meter measures the total amount of power of a signal. To do so, several sensors are employed. The most commonly is the use of a Schottky diode. Besides, it provides the better power reading among the other components.

Recently were created Universal Serial Bus (USB) Power Sensors. They can be used in a Vector Network Analyzer to calibrate its power measure.

3.2.3 Spectrum Analyzers

It provides a scalar measure across frequency, by measuring the amount of power contained into a narrow range of frequencies and then sweep the center frequency of the measurement.

Currently it commonly uses an IF Digitalization front-end like the one presented on 2.3.2.

[2] Also known as ΦM

3.2.4 Network Analyzers

Network Analyzers are very popular equipments used to characterize electrical networks. A Network Analyzer is an indispensable instrument in any radio laboratory due to its very wide utilization. It is used in research to measure the developed systems, it is used in production to automatically verify the assembled units and when combined with a set of antennas, it could became a radar.

In the past, two major types of Network Analyzers existed, the more affordable Scalar Network Analyzer (SNA) and the Vector Network Analyzer (VNA). While the SNA could only measure magnitude values the VNA could also measure phase. Currently, due to cost reduction the VNAs are nearly the only available choice as a brand new equipment. With the magnitude and phase values, the VNA are able to take linear component models, usually using S-Parameters (Scattering Parameters).

Scattering Parameters

S-Parameters are complex vector values that represent the ratio between two wave quantities. For example in a two port network there are four S-Parameter, as represented on figure 3.2. These, quantities are expressed as on equation 3.1.

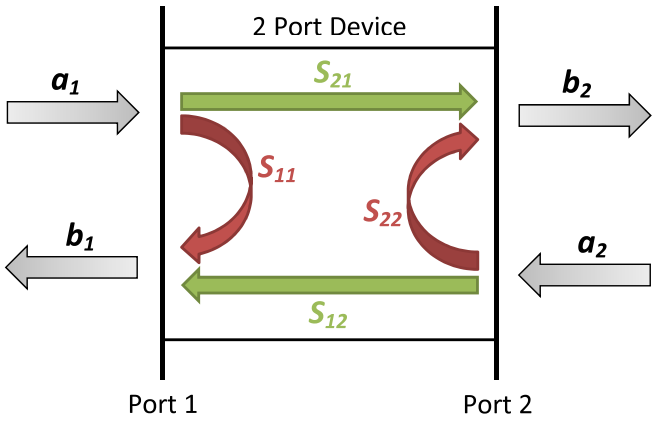


Figure 3.2: 2-Port Device S-Parameters

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \qquad S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \qquad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \qquad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{3.1}$$

As could be understood, two of the S-Parameters gave the ratio between the incident and the reflected waves on each port of the device – S_{11} and S_{22}, the other two gave the wave gain from one port to the other – S_{21} and S_{12}. This quantities are measured with one of the wave quantities at zero. To obtain a null wave quantity, the correspondent port must be adapted, i.e. the correspondent port must be terminated with a load equal to Z_0 – the reference characteristic impedance.

An adaptation is much more easy to perform at RF frequencies than the short circuit needed in the measurement of Z-Parameters, for example. Mainly, for this reason, at RF frequencies, S-Parameters are preferred to modeling RF components.

With S-Parameters a system of equations or an equivalent matrix could be created. This matrix characterizes the network and could be used as a model to build a system as an arrangement of several S-Parameters component blocks. S-Parameters could also characterize in the same way N-Port network devices. Once again, for a two-port device, the S-Parameters matrix is expressed on equation 3.2.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.2}$$

Architectures

To measure S-parameters, the need is to faithfully compare the several wave sets, in order to measure each quantity. To do it, the VNA uses several receivers, two per port, in a super-heterodyne architecture. Commonly, it has also incorporated a stimulus generator. A resume of its main blocks is shown on figure 3.3. Each receiver will down-convert a specific signal, the relation is the following: $1 - a_1$; $2 - b_1$; $3 - b_2$; $4 - a_2$.

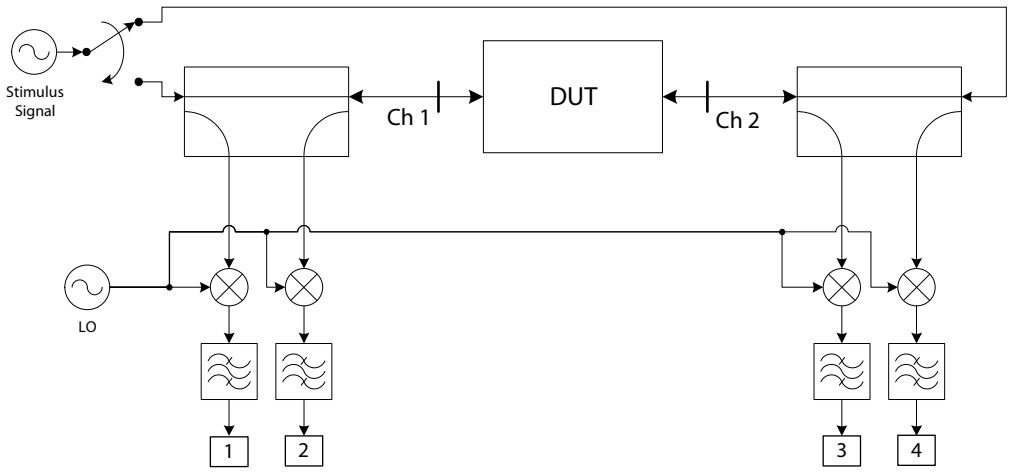


Figure 3.3: Architecture of a traditional VNA

From the ratio between the right read signals, it is possible to obtain the wanted S-Parameter. To achieve meaning results a calibration process must always be performed before a measurement. The calibration process intends to compensate for the instrument mismatches and to provide for a known measurement reference. If the calibration process is not performed the result obtain is meanless and don't provide a truth result at all. The calibration process is reviewed in more detail in section 5.4.

As a measurement example, to read the DUT S_{21} phase, the channel 3 have to be compared with the channel 1. The result phase is expressed in 3.2.4, as could be seen it is exactly the wanted quantity.

$$\phi_3 - \phi_1 = (\phi_{OUT_3} + \phi_{LO}) - (\phi_{IN_1} + \phi_{LO}) \iff \phi_3 - \phi_1 = \phi_{OUT_3} - \phi_{IN_1}$$

Actually, the VNA uses an IF Digitalization front-end. The ADC acquire the signal at an IF and the waves are compared each other digitally. To have an idea of the present VNAs performance, from the page 50 and 51 of [5] can be quoted:

The analog/digital converters used in modern network analyzers generally have a resolution of at least 14 bits. ... The analog mixer must generally be seen as the component limiting the dynamic range. ... Using a switchable amplifier, we can specifically target the levels in the analog section of the receiver and optimize them for the current RF input level.

As could be read in the upper citation, the use of a super-heterodyne architecture, in an IF Digitalization format, allows the use of ADCs with an high number of bits and so, the maximization of the instrument dynamic range. If an RF Digitalization architecture would be used, as on oscilloscopes, the dynamic range will be much lower.

Another great advantage of the super-heterodyne configuration is its capability to receive very high frequencies as well as very low. With this configuration the limiting upper frequency is virtually infinity[3]. Several arranges with switches and state-of-the-art components could be made in order to reach thousands of megahertz. Furthermore if a single conversion is not enough and if the upper frequency of the instrument is not enough, there are available front-end extensions to the VNA, which realize another down-conversion and grows up the instrument upper frequency.

An example of a State-of-the-art VNA operates from 10 MHz to 110 GHz and could be extended to 1,05 THz.

Besides the vector response over a frequency range, the VNA can be used as well to obtain power sweep measurements. The power sweep is intended to measure Figures of Merit such as, P1dB, AM-AM, AM-PM, among others.

In the past, another instrument appeared, the Microwave Transition Analyzer (MTA). Its functioning is based on time-domain reflectometry and it could measure a component frequency gain through its step response. However, the lack of user calibration, the demanding on an very good step generator to achieve good results and the limited accuracy causes this instrument to never achieve the success of the VNA.

Furthermore, Time-Domain Reflectometry is useful to locate faulty conditions in cables and in other transmission lines. It is now available using an high speed oscilloscopes with a pulse generator or incorporated as a function of VNAs, where the time-domain response is calculated through the Inverse Fourier Transform (IFT) process[15].

Nowadays the excitation is around non-linear characterization. The last improve in Network Analysis was the creation of large signal models and the instrument to measure them, the Large Signal Network Analyzer (LSNA).

Large Signal Network Analysis

Recently introduced by the instrumentation industry based on Polyharmonic Distortion Equations [16]. Two derivations of these equations were created, the X-Parameters by Agilent and the S-Functions by NMDG. The non-linear characterization is able to correctly modeling Amplifiers and the majority of passive devices including mixers, even in their non-linear region of operation.

Besides, it had been employed to perform Load-pull and Source-pull measurements[17]. These measurements allows to know the performance of the DUT under several load or source

[3]In the case of VNA the image issue, characteristic of super-heterodyne receivers, is not applicable. The input signal of the receiver is the DUT stimulus signal, which commonly is an one-tone signal.

impedances. With them is possible to choose the most suitable load or source impedance in order to pull the higher efficiency from the DUT.

3.3 Mixed-Domain Network Analyzer – The Proposed Instrument

The instrumentation industry, until now had been failed to present a fast and simple way to test an SDR or a mixed-domain component. Until now its suggestion employs a set of several instruments in an attempt to characterize an SDR[18]. The proposed instrument had the goal to fill this gap.

The idea is to build an instrument that could characterize a mixed-mode component from a radio engineering point of view, in order to give to the engineering community (that actually are in the pursuit to design SDRs) a direct way to test the overall radio performance of the entire SDR. This allows a quickly and easier mixed-domain radio design and so, the use of SDR system could be massified by the use of their strengths to reduce production costs and to improve quality of service.

To build such instrument, the start point must pass through the instruments that it is possible to find today in an RF lab. From all these instruments the closest equipment that already exist nowadays is the VNA. It characterize a component in frequency, but only on the analog domain. For this implementation the VNA was the start point. The way of thinking was always in order to add to this very well known piece of equipment the ability to operate in the digital domain too.

The quantities needed to characterize a mixed-domain component are very close to the ones measured on an actual VNA. For example, in an Analog-to-Digital Converter (ADC), the port 1 is analog and the port 2 is digital, thus the measured quantities needed to produce a model are the traditional $S_{11}(\omega)$ and the gain of the DUT expressed like the $S_{21}(\omega)$ on an analog component [2].

In this work, the traditional VNA front-end architecture was adopted to the instrument's analog port and the LA like front-end to the digital port.

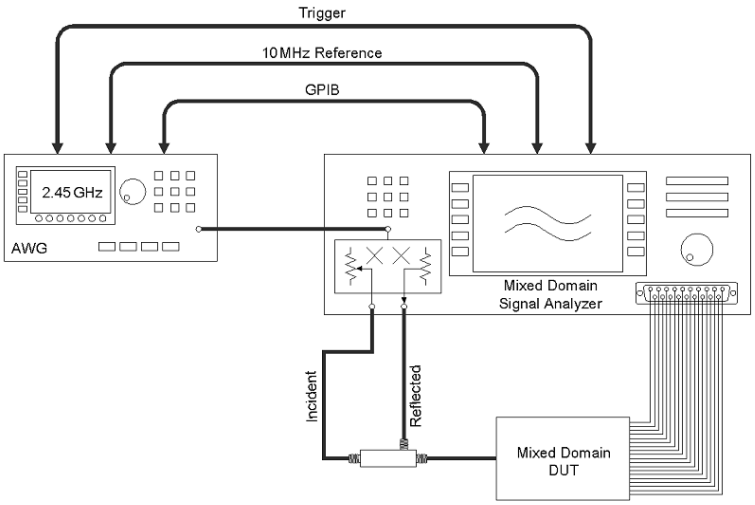


Figure 3.4: Proposed Instrument Illustration, from [2]

Chapter 4

Implementation

4.1 Overview

The baseline to build the proposed instrument was presented in the end of the last chapter. So it will be necessary to build two front-ends, one based on the traditional VNA front-end and another based on the less well known LA front-end.

Due to the mixed-domain nature of the measurement is impossible to affect both the signals, digital and analog, with the same LO. This is the biggest problem that we have to resolve to take accurate phase measurements. For this implementation, in demand of simplicity, it was decided to construct a one port VNA like analog front-end and one port digital front-end. The synchronism issues will be taken care later. The figure 4.1 is an overview description of the instrument and in this chapter will be presented the components chosen to build it. To easily build and test the entire instrument, it was divided into two stages, the analog ant the digital stage.

The analog stage covers all the analog components of the equipment until the ADC. Like on traditional VNAs the incident and the reflected signal will be compared each other, which means both the paths from the signal separation, should be closely similar. So the components used will be the same on the two paths. The path that receives the incident signal will be refereed from now on, as the Incident Path and the path that receives the reflected signal as Reflect Path.

The digital stage incorporates the ADC, its peripherals and the Digital Unit, which incorporates the Digital Receiver and the Digital Generator.

To build the analyzer proposed some goals need to be defined. Once it was intended to test SDR, the most obvious band that it has to cover is the one that as expected to be assigned in Portugal to SDR systems which covers part of the electromagnetic spectrum that are actually assigned to analog TV in the UHF band (470-862 MHz) [21]. Although the most spectra that the equipment covers the better this prototype will be, so the goal is to covers from the upper GSM band (925-960 MHz), down through the actual Portuguese Digital TV band (TDT) (750-758 MHz), include the 868 and 433 MHz ISM bands, and even the FM band(88-108 MHz).

The majority of the ADCs commercial available have an internal voltage reference of 2 Vpp, which is 10 dBm for a 50 Ω load impedance. The suggested goal to the maximum test power that the instrument should be able to handle is higher than the 10 dBm, let's say 15 dBm. This way the instrument will be able to characterize the majority of the ADCs in

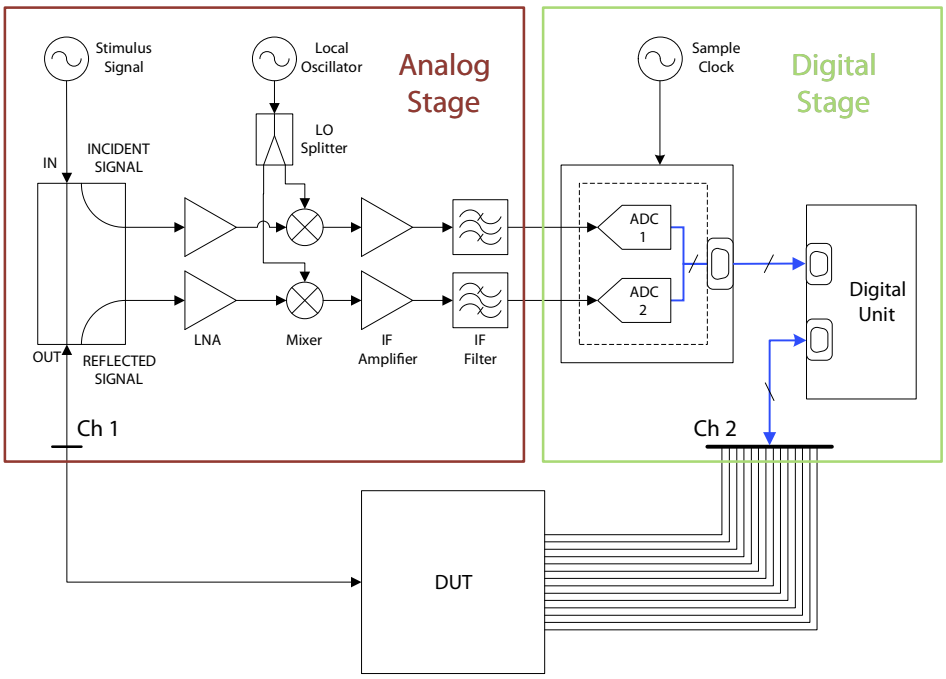


Figure 4.1: Block Diagram of the proposed Instrument

their clipping zone.

In the end of the analog stage, the two paths need to be digitized. To that purpose a commercial ADC needs to be used. Thus, it will more likely have a common 2 Vpp reference, which means it will clip at 10 dBm. As said before the goal is to have a maximum stimulus signal of 15 dBm. This way the overall gain system needs to be -5 dB.

With the block diagram sketched on figure 4.1 and the main goals defined, it's now time to choose for each block the right commercial component to do the job. In order to maintain the price of the equipment as low as possible, each component should already exist in stock at Instituto de Telecomunicações (IT), or it should cost as less as possible. Furthermore, the equipment must perform at least the minimum specifications described previously.

There is another limitation, when the components to build the proposed instrument have to be chosen, the components must be connector components, preferentially with Sub-Miniature version A (SMA) connectors, because it is the most usually kind of connector and so the other components will likely connect directly to it. If the component is an Integrated Circuit (IC), it has to be possible to solder on it. Thus, it has to be an DIP package or a Surface Mount Device (SMD) package, like SOT, SOIC or TQFP, with a minimum pitch of 0,5 mm, with leads and without solder area underneath the chip.

4.2 Analog Stage

4.2.1 Signal Separation

The first block of the instrument's analog signal chain is a signal separation block, it should separate the incident wave from the reflected wave, in a way that the equipment could compare both the waves. To do this three major types of components are traditional used in VNAs: bridges, or couplers.

The first ones have a response from DC to many GHz due to their resistive nature, however both have much more attenuation on the signal's direct path to the DUT. Couplers instead, due to them non-resistive characteristic, are band limited and are only available above some kHz, however they have very low attenuation through the main signal path, and very good isolation and directivity.

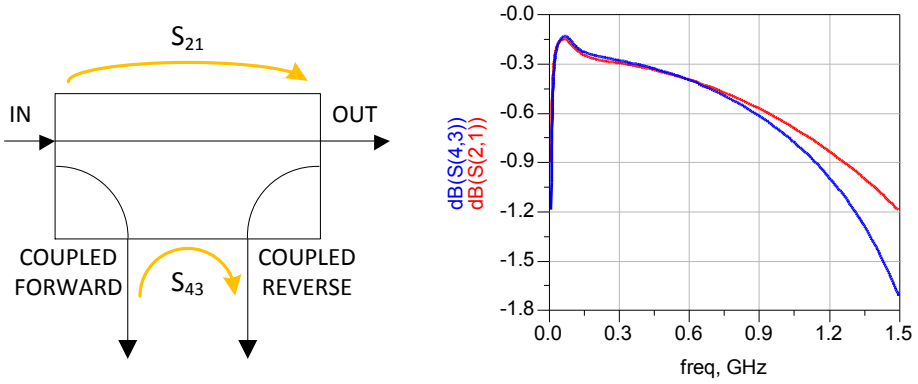
Just like the majority of the VNAs available today, the inferior band limit goal for the proposed instrument, doesn't have to be DC, so the choice goes to the coupler. In this main component category are two different types of couplers, bi-directional couplers that can take, in one component, a small amount of the incident wave and a small amount of the reflected wave (bi-directional coupler are 4 port devices) and directional couplers that only take a small amount of the wave in one direction and the other direction was isolated (directional couplers are 3 port devices). In this matter the choice was made by a bi-directional coupler of Mini-Circuits, the ZFBDC20-13HP-S+, it has the following specifications, from [22]:

- 50 Ω
- 40 to 1000 MHz
- 0.4 dB mainline loss, typ.
- 20 dB Coupling, typ.
- 20 dB Directivity, typ.
- Rugged shielded case with SMA connectors
- Up to 20 W
- Price = $75.95

In the simulation of the coupler's characteristics using the Advanced Design System (ADS) software with the S-parameters file available on the Mini-Circuits website, a problem that the author wasn't aware before and is common to bi-directional couplers was noticed. The isolation between coupled forward port and coupled reverse port, S_{43} depicted on figure 4.2 and S_{34} was almost 0 dB, similarly to the main path. Using two directional couplers this problem would not exist, however the utilization of just one component instead of two appears to be more cost effective, and with calibration the problem mentioned before will be exceeded, for certain. So the choice for this component was maintained.

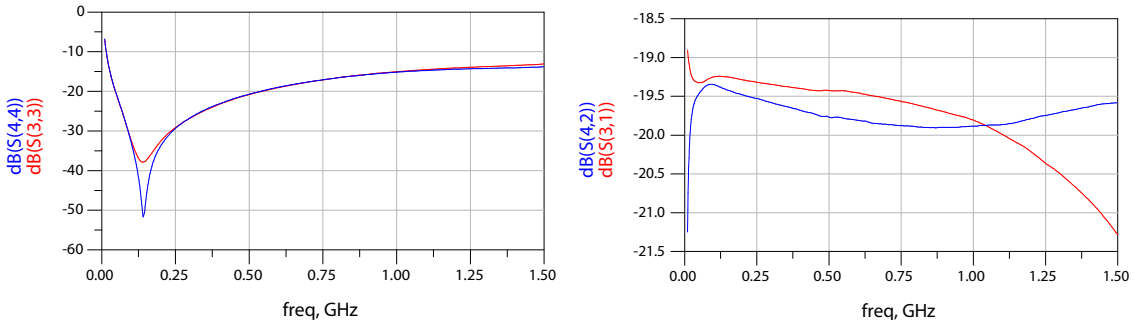
The measures of the coupler verify the values presented in the datasheet and the results obtained by simulation. The S_{33} and S_{44} in figure 4.3a and the S_{31} and S_{42} in figure 4.3b are also depicted.

Lately was noticed that, due to the much more extensive list of models of directional couplers that exist in the market, with two directional couplers the work band could be



(a) S_{21} and S_{43} on Bi-Directional Couplers (b) S_{21} and S_{43} from simulation

Figure 4.2



(a) S_{33} and S_{44} (b) S_{31} and S_{42}

Figure 4.3: Bi-Directional Coupler Simulation Results from 10 MHz to 1,5 GHz

extended and the previously problem avoid. Nevertheless, the bi-directional coupler chose has characteristics that could meet the requirements and was very cost effective.

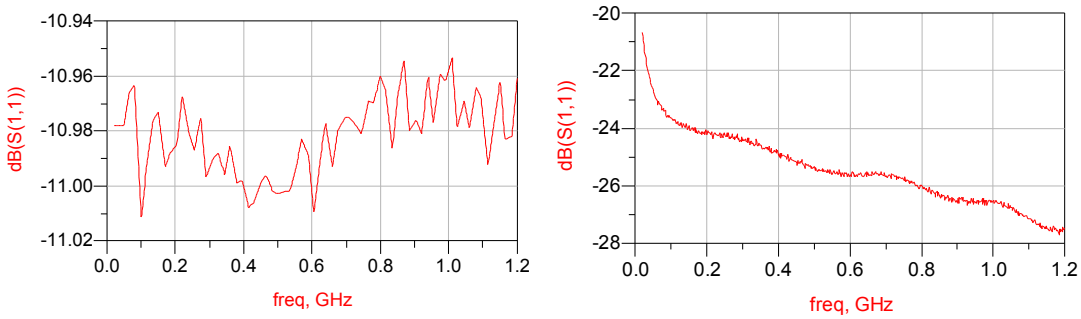
4.2.2 First Amplifier - LNA

The first amplifier in the signal chain was supposed to gave gain to both signals. For example, the incident wave will be attenuated at the coupler by 20 dB and then amplified by this component, and then attenuated again by the next components in the signal chain. So this amplifier should deliver enough gain to the signal so it can reach the other amplifier strong enough, introducing as less noise as it can (which means it should has the lesser NF possible, so an Low Noise Amplifier (LNA) was chosen) and in addiction it can't distort the signal when input power to the DUT was set to maximum. Evidently the amplifier must work in all the bandwidth of the equipment, that until now is at least from 40 to 1000 MHz.

With the previously goals in mind, the choice for this LNA was between two amplifiers that already exist in IT's stock, the MAN-2 and ERA-4, both from Mini-Circuits. It is important to refer that the ERA-4 is an evaluation board model, so its functioning was guaranteed in all the work bandwidth, the MAN-2 has all the adaptations and polarizations inside its case and so it's work bandwidth was guaranteed too.

By the datasheets of the two amplifiers ERA-4[23] and MAN-2[24], the ERA-4 is an obvious winner, it has higher bandwidth, lower NF, higher Output P1dB and equally good RL. The only disadvantage lies in a lower gain than the MAN-2, although its gain is enough for the purpose.

However from the simulation models provided from Mini-Circuits to its ERA-4 model, the Return Loss (RL) of the ERA-4 amplifier wasn't so good as they are depicted on the datasheet. The Return Loss was just 11 dB, as depicted on figure 4.4a, which was too low for the needs. Because, taking into account that this first amplifier is to be placed right after the bi-directional coupler chosen and the coupler has the S_{43} issue mentioned, the amplifier chose must have a good RL, let's say at least higher than 20 dB. Thus, with the values from the simulation file the ERA-4 can't be the choice any more...



(a) ERA-4 RL from simulation

(b) ERA-4 RL from VNA measure

Figure 4.4: ERA-4 Return Loss

Nevertheless as the amplifier already exist at IT, the decision was to measure its real performance with a VNA and the results shown on figure 4.4b, are impressive. The actual RL are the one that are registered on the datasheet and not, as expected, the results obtained by the simulation file. By some reason the simulation file retrieved from the Mini-Circuits website some error on the RL, and for worst, which is somehow strange. After all, good news, the conclusion of the good Return Loss apart with the better performance mentioned before, finally decide the choice on the ERA-4.

Its specifications[23] are depicted bellow:

- DC-4 GHz
- Gain = 14,2 dB @ 1 GHz
- Output P1dB = 17,3 dBm @ 1 GHz
- Output IP_3 (Third-order Intercept Point) = 35 dBm @ 1 GHz
- NF = 4,2 dB @ 1 GHz
- Input RL = 30 dB @ 2 GHz
- Single voltage supply
- Internally matched to 50 Ω

The Gain at the work bandwidth and the P1dB at 1 GHz were measured also. They are depicted in figures 4.5 and 4.6.

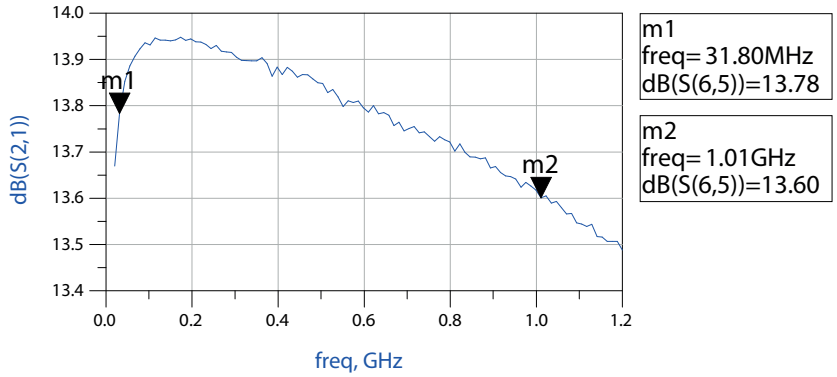


Figure 4.5: ERA-4 Simulated and Measured Gain

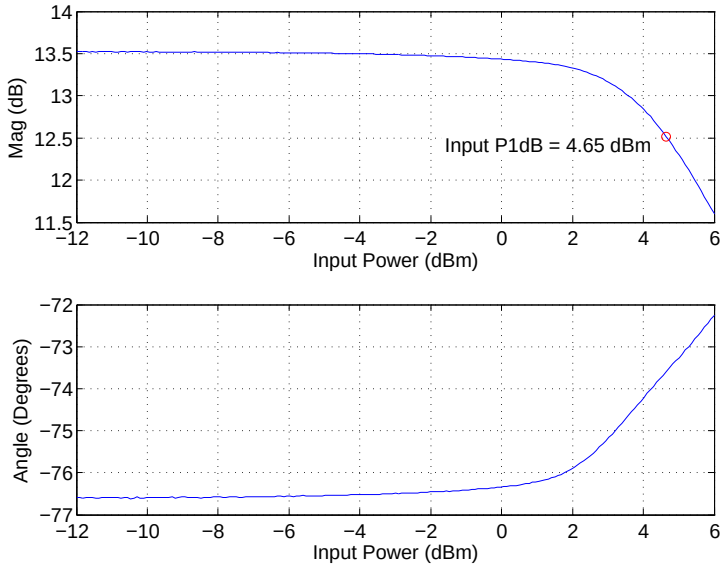


Figure 4.6: ERA-4 Measured Input P1dB at 1 GHz

With the ERA-4 measurement results and with the coupler's S-Parameters, a simulation of the Directivity on the Direct and on the Reverse path was done. Its results are depicted on figure 4.7. In both paths the directivity is always better than 15 dB, from 40 MHz to 1 GHz. In the reverse path the directivity reach very high values, higher than 30 dB at the center of the band.

4.2.3 Mixer

The next component on the chain is a mixer to down-convert the incident and the reflected signal. The main specifications that the mixer has to ensure are: preserve the maximum

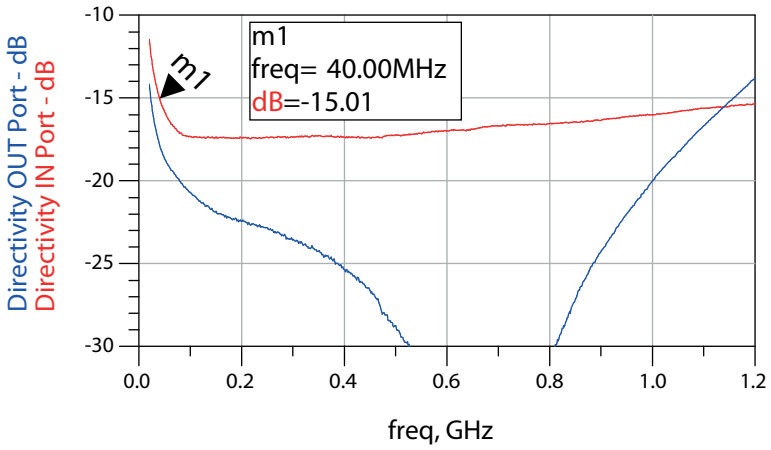


Figure 4.7: Simulated Directivity from 20 MHz to 1 GHz

bandwidth available until now, have the higher P1dB possible, have the lower attenuation possible and as always, have the lower cost possible.

The bandwidth are limited by the worst component from 40 to 1000 MHz. The isolation between the ports of the mixer must be as high as possible. The two components behind the mixer produce a gain of -5,8 dB. Disregarding the coupler P1dB, until this point the system input P1dB is 22,9 dBm. In order to maintain the initial goal of 15 dBm for the instrument maximum input power, the input P1dB of the mixer has to be higher than 10 dBm, which could be very hard to find.

The mixer chosen was the ZX05-5+ from Mini-Circuits. It was the mixer that best suited our needs with lower cost. Its features, according with the datasheet[25] are:

- 5 to 1500 MHz
- LO power = 4 to 10 dBm
- RF max power = 16,9 dBm
- L = 7 dB
- Input IP_3 = 15 dBm
- Price = $37.95

The traditional rule of thumb for the relation between the IP_3 and the P1dB, on this kind of components, says that the P1dB is 10 to 12 dB lower than the IP_3. This way, using that rule it was possible to calculate and predict the expected Input P1dB for the global receiver. The input P1dB used on that calculations was 3 dBm.

By the use of the technique presented on A, the mixer P1dB was measured with an 800 MHz RF signal and a 860 MHz LO signal at 7 dBm, to produce the same conversion used on the system with 60 MHz IF. The result obtained can be depicted on figure 4.8. The Input P1dB of 1,63 dBm is even lower than the assumed by more than 1 dB.

So, the input P1dB of the mixer will dictate the maximum input power of the equipment, which is lower than the initial goal. But, for now this mixer was the best commitment.

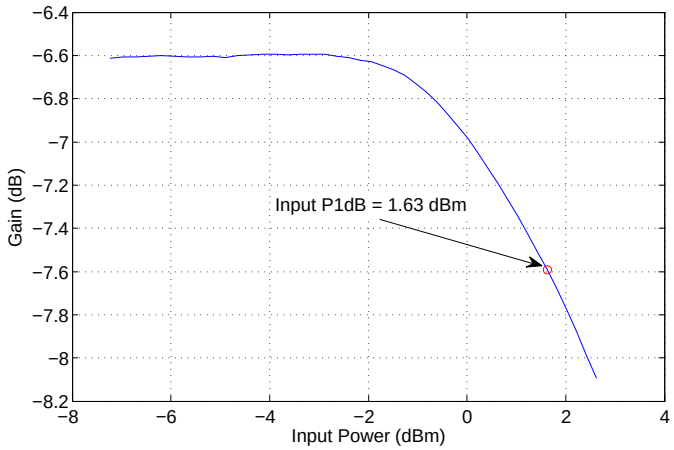


Figure 4.8: Mixer Measured Input P1dB at 800 MHz

4.2.4 IF filter

Considering that in the end the signal will be digitized by an ADC with a sample rate of 80 Mega-Samples Per Second (MSPS), the Intermediate Frequency was set on the center of the second Nyquist zone, at 60 MHz. The bandwidth of the filter isn't defined yet, but it has to be less than 40 MHz in order to cancel the over position of spectrum after the sampling process and it should be as larger as possible in order to receive signals with more than one tone or even multi-sines. The large bandwidth could be helpful to understand the impact of these more complex signals in the DUT.

With this considerations the first step of the design was to understand the impact of the transition band and the stop band attenuation level in order to specify this characteristics too. From the figure 4.9 can be denoted that after the sampling process the pass band will be positioned over the correspond band in other Nyquist zones, represented by green on the figure. To maintain the result signal as pure as possible the attenuation on this zones should be higher enough so, 40 dB was specified to the stop band. To avoid over-position of the desire signal the bandwidth of the transition zones can be twice the non used bandwidth of the pass band. In other words if the higher cut frequency of the filter began at 70 MHz the stop band or the necessary attenuation level should began at 90 MHz to avoid degradation of the signal at the pass band.

There are several types with different filter responses. In order to maximize the bandwidth and maximize the attenuation at the stop band, the design of an Elliptic filter was selected. Many tools are available to design filters, the most traditional of all is to follow the tabled normalized values that can be found on vast literature, use them to produce a normalized low pass filter and by successive transformations achieve the wanted filter. To follow this method for the elliptic class of filters the [26] and [27] can be used to provide the normalized table values.

The approach taken on this design was quite different and the utility Filter DesignGuide of the ADS was used instead. Using this methodology was possible to interactivity change the filter parameters in order to achieve a filter that best suits the characteristics defined previous and at the same time was practical to implement using components that already exists on IT's stock. Therefore to take the transfer function of the filter as close as possible

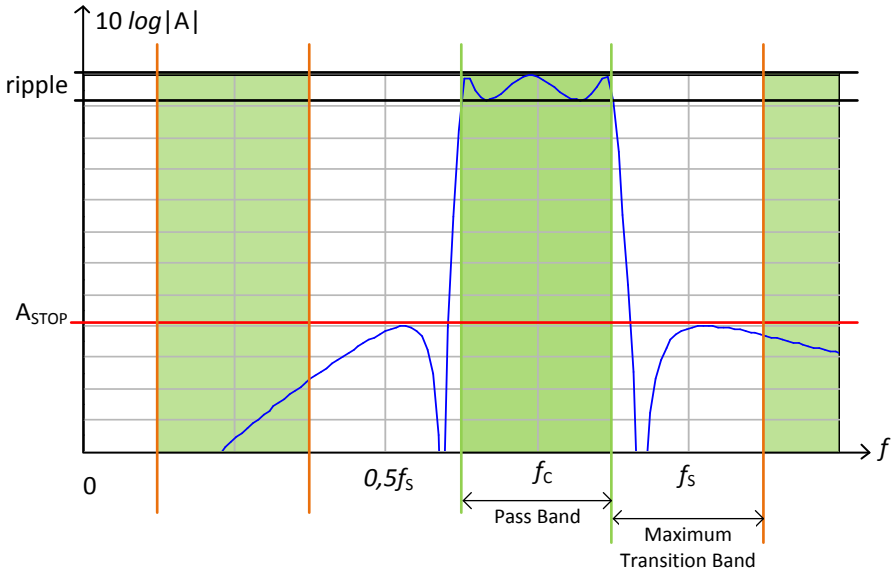


Figure 4.9: Transition band of the IF filter – Freedom degree

to the calculated one, the components value returned by the software should respect three essential goals:

1. Have a resonance frequency, at least 5 times greater than the work frequency, essentially on large value inductors that have lower resonance frequencies;
2. Have an impedance at work frequency grater than 10 Ω, essentially on higher value capacitors in order to it's parasitic resistive part don't be the prevailing part;
3. Have values close to the standard ones.

After some interactions, the filter final schematic shown on the figure 4.10, was achieved. The Printed Circuit Board (PCB) layout of the filter is presented on the Appendix.

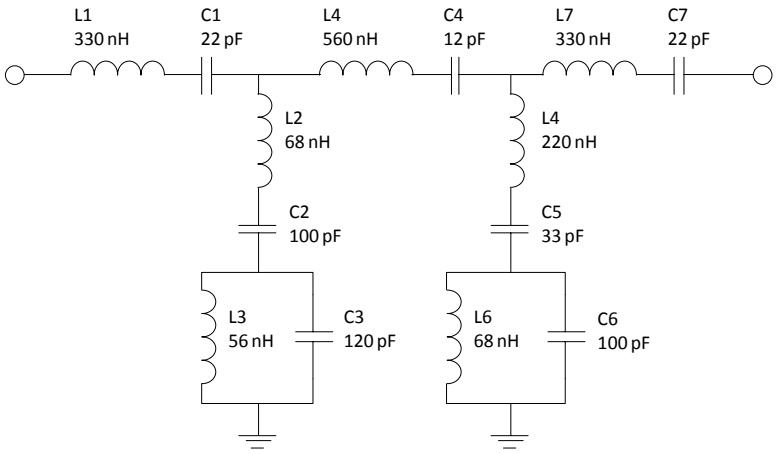


Figure 4.10: IF filter schematic

Results

The frequency response of the simulated filter and the frequency response of the two filters implemented are depicted from 10 to 1000 MHz on the figure 4.12 and with detail, from 20 to 120 MHz, on figure 4.11.

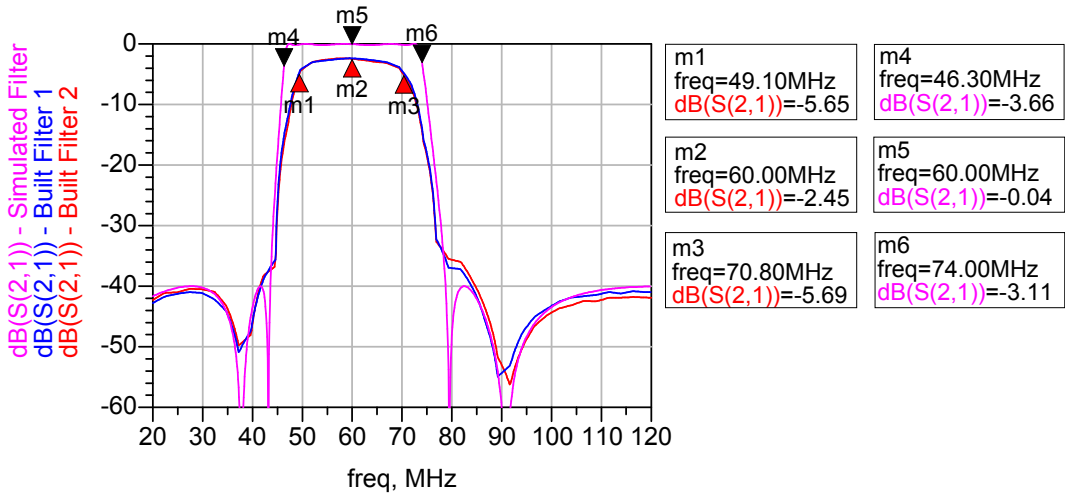


Figure 4.11: IF filter response comparison (detail), from 20 to 120 MHz

As can be seen on figure 4.11 the filter has a close response to the simulated, the stop band has similar attenuation and the transition band is fast dropping down. Apart from the higher attenuation at the pass band of about 3 dB and the slightly lower bandwidth of about 6 MHz, the curve response follows the simulated very well.

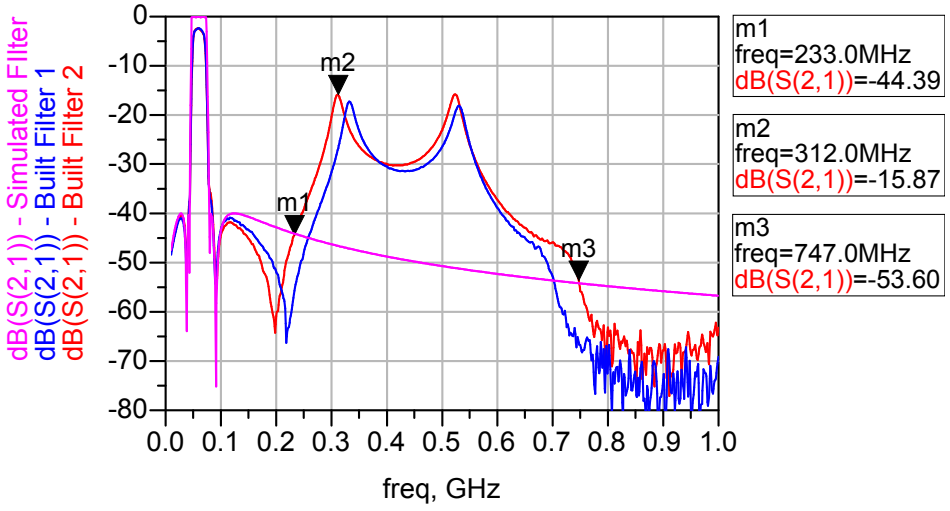


Figure 4.12: IF filter response comparison, from 20 to 1000 MHz

However in the figure 4.12 can be denoted that the attenuation of the filter rises again at 200 MHz, due to the frequency resonance of the components that change their behaviour and degrades the theoretical curve response. To minimize this effect another filter has to

been added, this filter can be a low pass filter and it's intended was only to cancel the lack of attenuation at stop band after the 200 MHz.

Another miss alignment are the differences between the two filters implemented. Once again as seen on figure 4.12, the curves in blue and red are quite different, at least after the 100 MHz. This behaviour can be explained once the components used on the two filters aren't the same, this means that the components of the first filter aren't from the same manufacturer of the components from the second filter, although the same value of components were been used. This happens because one of the first two filters produced was damaged on the measure process and so another one have to be produced, but then another components have to be bought. Nevertheless this wasn't a big issue, the difference between the two filters can be disregarded because they appear only outside the band of interest.

4.2.5 IF Amplifier

After the IF filter select the band of interest, the signal needs to get more strength. The goal is to have a total gain in all the path until the ADC of -5 dB. To accomplish it, another amplifier needs to be added. This amplifier will only work at IF frequency, in the band of 50 to 70 MHz, as seen before.

Until this point, considering the attenuation of the previous IF filter, the signal of interest is attenuated 15,8 dB. So, the main goals for this amplifier are:

- Gain at least of 15,8 dB;
- High P1dB and IP_3;
- Work at IF band.

Therefore availing the amplifiers available from another projects of the author, the amplifier chosen was the Avago ABA53563. Its features, from [28], are:

- DC – 3,5 GHz
- Gain = 21,5 dB @ 2 GHz
- P1dB = 12,7 dBm @ 2 GHz
- Output IP_3 = 22,9 dBm @ 2 GHz
- NF = 3,5 dB @ 2 GHz
- Single 5 V voltage supply
- Internally matched to 50 Ω
- Available on SOT-363 package

A board was design and build. The schematic can be seen in 4.13 and the final PCB can be seen in figure C.3.

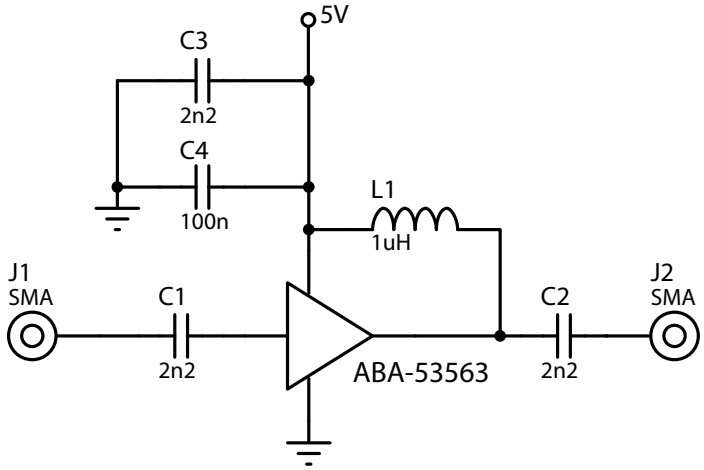


Figure 4.13: ABA53563 Schematic Board

Results

As can be seen on figure 4.14 the built amplifier board has the predicted frequency response. Only at 571,8 MHz the gain drops down about 2 dB and then rises again to the normal gain, as shown on the marker m3. This behaviour is most certainly due to the resonance frequency of the coupling components used on the board. Nevertheless in the work band, from 50 to 70 MHz, the gain is almost constant and powerful enough.

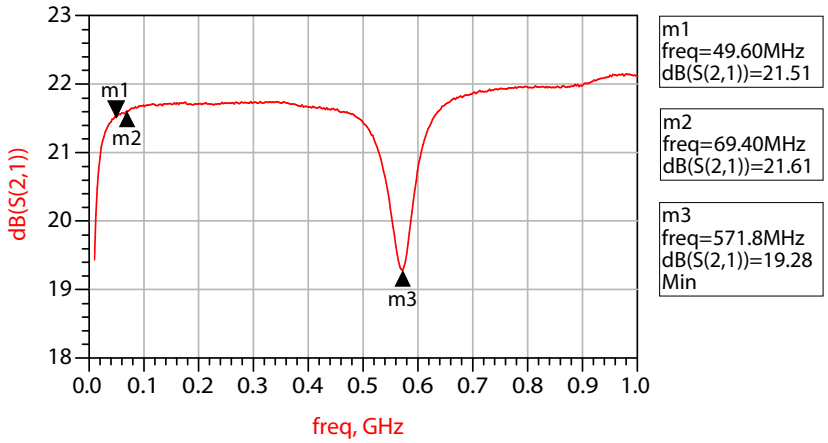


Figure 4.14: ABA53563 Frequency Response

The P1dB of the amplifier board was also measured and the results are depicted on 4.15.

From the power sweep results, it was possible to realize the input power level, from where the amplifier began to generate distortion. From the gain traces, it was possible to say that around -15 dBm the amplifier began to distort, which make sense, since its Output Third-order Intercept Point (OIP3) is 22,9 dBm. This OIP3 level corresponds to an Input Third-order Intercept Point (IIP3) of 1 dBm so, at -15 dBm input power the Intermodulation Ratio (IMR) is 32 dB and the Third-Order Intermodulation (IM3) product doesn't have impact on the output signal yet. But from then on, the IMR began to decrease with a rate of 2 dB per 1 dB increased in input power. This phenomena leads to a negative impact of the IM3

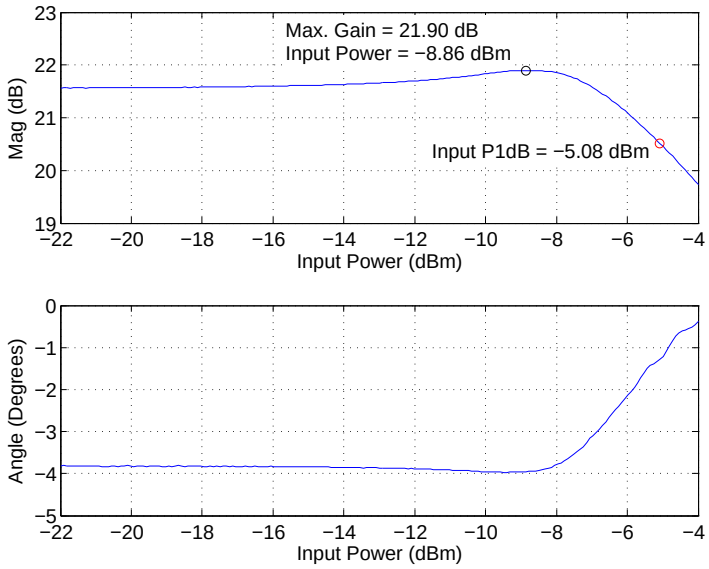


Figure 4.15: ABA53563 Measured Input P1dB at 60 MHz

product on the output signal by expanding the gain and modify the phase delay, generating Intermodulation Distortion (IMD).

The expansion effect pull the P1dB to a level proximal of the IP_3 and so the amplifier began to distort the input signal too soon. The initial goal is to have a maximum input power on the system of 15 dBm distortion free. After perform cascade calculations to the global system with the ABA53563 in the chain, the final IIP3 was too much decreased by this amplifier. Which implies that the amplifier will contribute to the soon appearance of IMD. Even though the goal will not be accomplished due to the low mixer IIP3, the IF amplifier shouldn't have impact in the final result. The mixer should be the limiting component in this topic.

The author until the time of this evaluation did not have the sensibility to evaluate a component power response from its IP_3, with this event the IP_3 figure of merit shows itself as an important factor when the objective of the amplifier is to be distortion free.

4.2.6 Redefine IF Amplifier

In order to decrease the influence of the IF amplifier in the global system IIP3 and improve the maximum input power of the system without distortion, another IF amplifier, with a higher IP_3, has to be chosen.

The IC chosen was the ADL5536, from Analog Devices. Its characteristics are listed below [29]:

- 20 MHz – 1 GHz
- Gain = 20,1 dB @ 70 MHz
- P1dB = 19,6 dBm @ 70 MHz

- Output IP_3 = 41 dBm @ 70 MHz
- NF = 2,4 dB @ 2 GHz
- Single 5 V voltage supply
- Internally matched to 50 Ω
- Available on SOT-89 package

The OIP3 difference is massive. This OIP3 corresponds to 20,9 dBm IIP3, which assures for certain that the limiting component to the global system IIP3 is the mixer and the impact of the IF amplifier is very low. The other characteristics of the amplifier are suitable to the purposes also. Only the poor RL at both ports and the higher cost are disadvantages to the ADL5536 (for 1000+ quantities, the ABA53563 costs 0,4$, while the ADL5536 costs 2,4$).

Once again a board was produced taking in mind the work frequency. Its schematic is shown in figure 4.16, the PCB can be depicted on C.4.

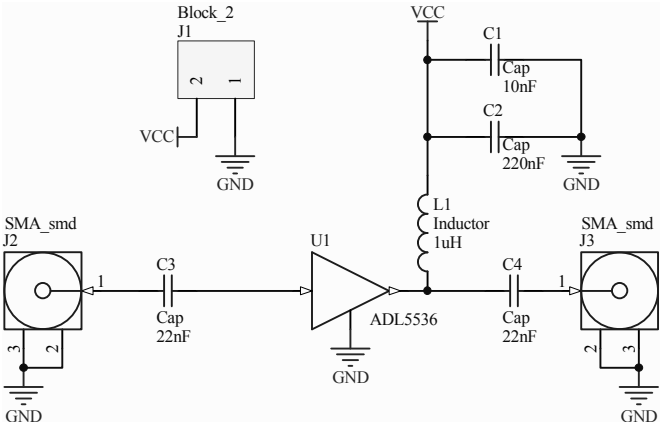


Figure 4.16: Schematic of the ADL5536 IF Amplifier

Results

The board frequency response from 20 to 1000 MHz is depicted on figure 4.17. The gain from 20 to 100 MHz is slightly above 20 dB and it is almost flat, as necessary. The RL in both ports was quite good too, even better than the simulated, from 50 to 1000 MHz it is always better than 17 dB.

The result for its P1dB is depicted on figure 4.18. From the power sweep gain traces, no distortion could be denoted at least before the 10 dBm input power. The point where the distortion began was improved at least 10 dB and no gain expansion is present on this amplifier.

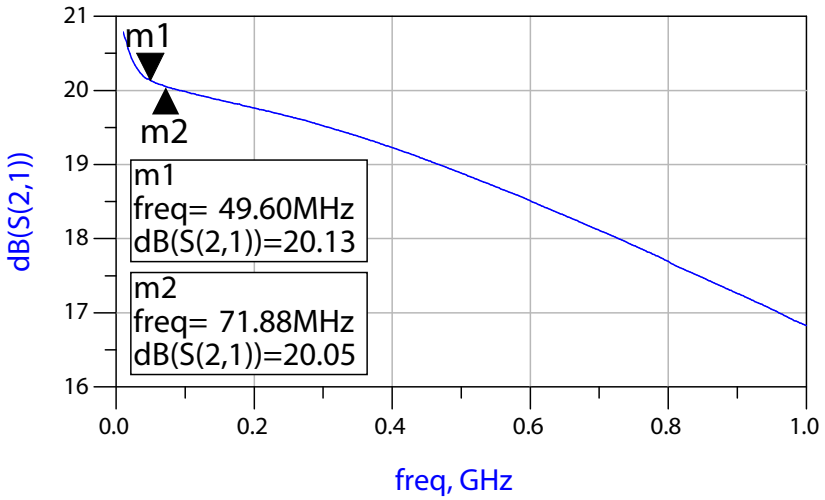


Figure 4.17: Frequency Responce of the IF Amplifier – ADL5536

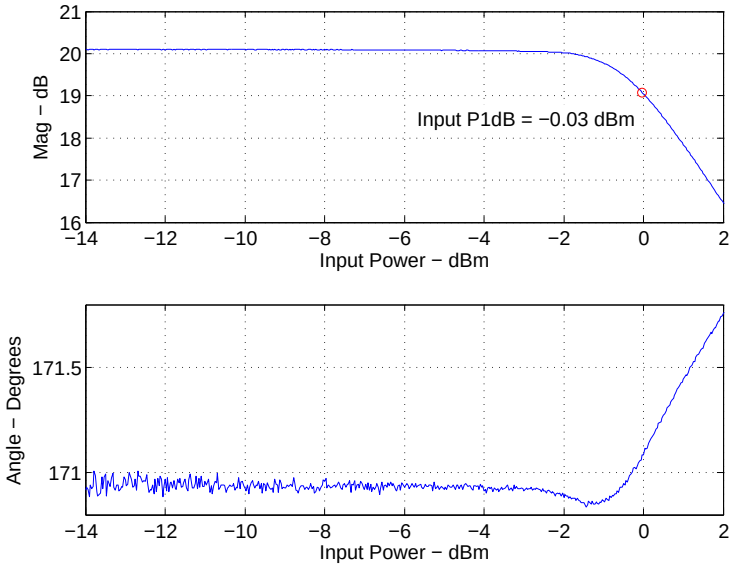


Figure 4.18: ADL5536 Measured input P1dB at 60 MHz

4.2.7 Low-Pass Filter

In order to maintain the Rejection Level high enough in all the rejection band an additional Low-Pass Filter (LPF) has to be used to attenuate the response between the 200 MHz and 700 MHz. To do that an 3rd order Butterword LPF was projected using once again the utility on ADS.

The procedure was much closer to the previous one for the Band-Pass Filter (BPF). The fixed parameter of the filter was the stop band, that as to be at least 25 dB at 300 MHz in order to attenuate the first unwanted peak of the IF filter response (the marker m3 in figure 4.12), which has approximately -15 dB at 312 MHz. The remain parameters were interactively

changed until an appropriate design was founded. The final circuit with the commercial values already chosen is depicted on figure 4.19.

The measure and simulation of the LPF are depicted on figure 4.20a. The response of the filter was closely similar to the simulated one. The PCB layout is again presented on the Appendix.

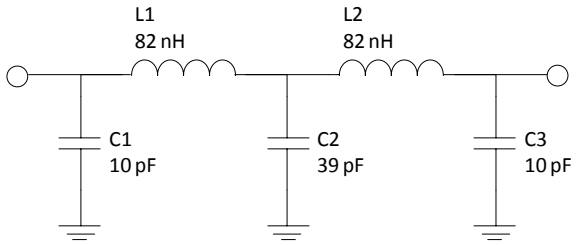
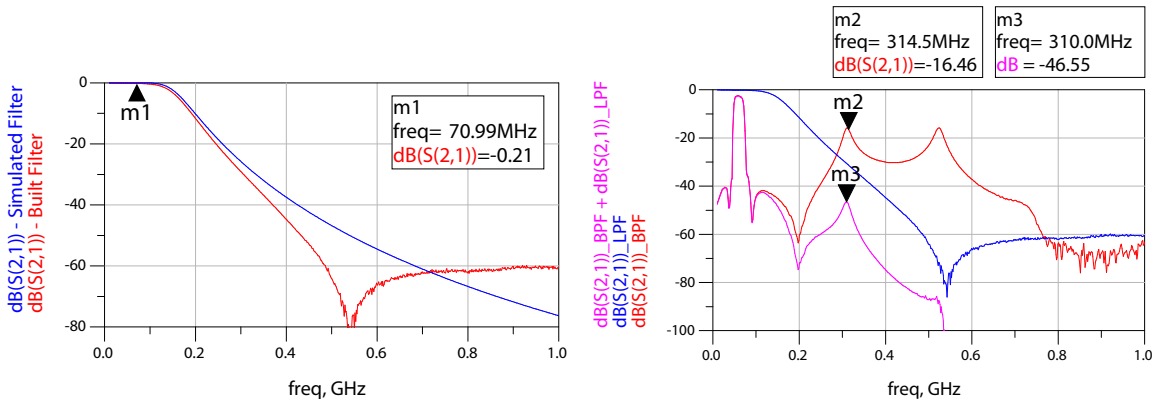


Figure 4.19: Low-Pass filter schematic

The results of the filter were quite good, with an attenuation of only 0,2 dB at the band of interest (50-70 MHz). In the figure 4.20b were depicted the frequency response of the LPF, the BPF and the arithmetic sum of the two magnitude responses. From the last one, is possible to see that the attenuation of the LPF, at the frequency of the unwanted BPF peak, is enough to maintain the rejection level in all the stop band below 40 dB.



(a) Simulated and Measured response comparison

(b) Comparison with BPF frequency response

Figure 4.20: Low-Pass Filter frequency response, from 10 to 1000 MHz

4.2.8 IF Stage Arrangement

In order to understand the order of interaction between the two filters, various tests were done, with them two next to each other and separated by the IF amplifier. So, two arrangement could be chose, for the IF stage:

1. Amplifier-BPF-LPF
2. BPF-Amplifier-LPF

In the figure 4.21 are the results for the frequency response of the two previous arrangements. Almost insignificant differences were found. With the arrangement 1 can be denoted a low interaction level that makes the peak indicated by the marker m1 at 178,4 MHz, but it has an attenuation high enough to be disregarded.

From the return loss results shown on figure 4.22, the arrangement 1 has the better result with, in the worst case, 3 dB RL out of the IF band. Further, a power sweep had been also performed, even it is not shown here, the result with 1 was again much better. So the arrangement 1 is the best choice and it was the one used. In figure 4.23 are depicted the final phase delay results.

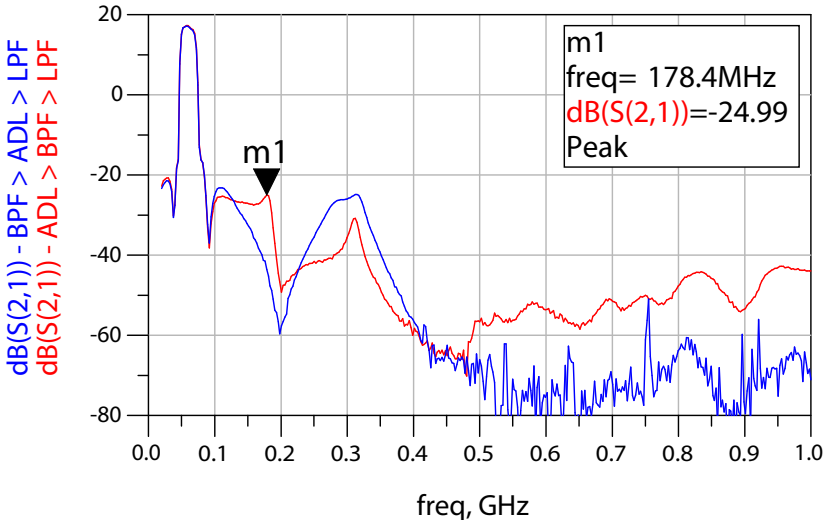


Figure 4.21: IF stage arranges, frequency response comparison

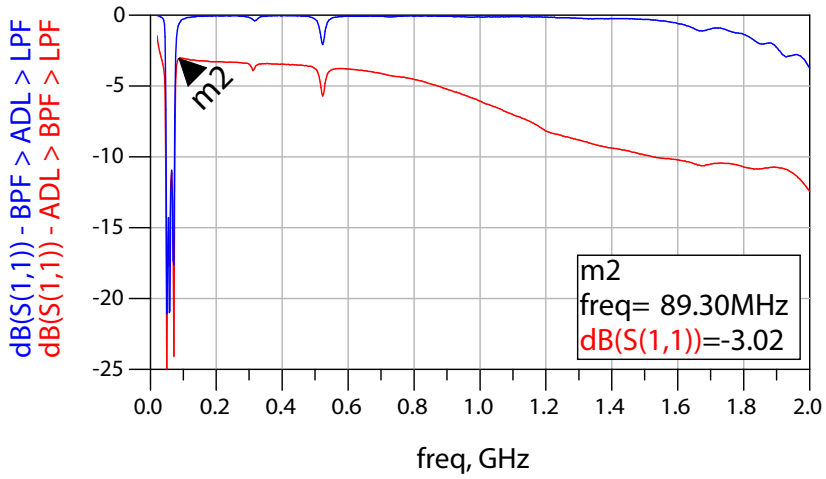
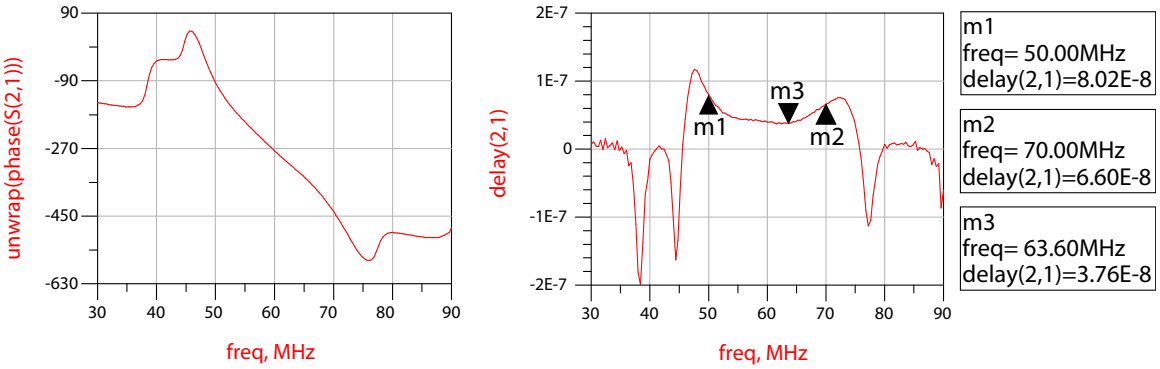


Figure 4.22: IF stage arranges, Return Loss comparison



(a) Phase (b) Delay

Figure 4.23 IF stage arranges phase and delay, from 30 to 90 MHz

4.2.9 Local Oscillator Splitter

The two analog paths are two receivers based on the superheterodyne principle. This way the mixer will down-convert the RF signal to a fixed IF. The chosen conversion to do this task was $f_{LO} - f_{RF}$, so the Local Oscillator (LO) signal will always be 60 MHz higher than the RF signal.

In order to down-convert both, the incident and reflected signals with the same LO, a Splitter is needed. It will split the LO signal from a generator and feed the two mixers with approximately the same LO. This splitter has to cover the entire work band and has to handle the power needed by the mixer to work properly. The amount of power intended to feed the mixers was 7 dBm and the maximum power available on the output of the lab signal generators was 20 dBm. Thus, the following goals has to be respected:

- Bandwidth at least from 100 to 1060 MHz
- Max. Attenuation = 13 dBm
- Max. Input Power = 7 dBm + attenuation
- Low cost

As the bandwidth specified for the splitter isn't too large, an non-resistive splitter was chosen in order to have a lower attenuation and a lower price. The splitter chosen was the Mini-Circuits ZX10-2-12-S+. Its features, from [30], are:

- 2 to 1200 MHz
- Low Insertion Loss 3,5 dB typ.
- Amplitude Unbalance 0,5 dB max.
- Phase Unbalance 3° max.
- Max. Power Input (as a splitter) 0,5 W - 27 dBm
- Price $24.95

4.2.10 System Evaluation

In order to evaluate the global system performance to assure its ability to fulfil the equipment measure goals several tests were performed and compared to what have been calculated. Therefore some changes were made to the global design in order to improve its performance.

Using a calculation sheet and the software ADS the global gain, global NF, input P1dB and input IP_3 of the system were calculated. The cumulative results of the entire analog stage are shown on table 4.1.

Gain (dB)	NF (dB)	Input P1dB (dBm)	Input IP3 (dBm)
4,10	24,66	7,17	20,27

Table 4.1: Cascade Analysis - version 1

At this point, the total gain of the system is equal to 4,1 dB, higher than the goal, so there are still some degree of freedom and some trade for this gain can be done yet.

The first change in the system comes from an effect already cared before, the low system IIP3. In order to avoid distortion in all the system dynamic range, the IMR should always be higher than 40 dB. The IIP3 of the system is now set in 19,83 dBm, which is too low considering the wanted input power of 15 dBm, the result is an IMR of only 10 dB. As said before the system was designed in order to have the mixer as the limiting component in this topic. However, achieve the initial goal is not possible without further alteration of the system. So to minimize those alterations, it was decided to change the initial goal to a maximum input power of 5 dBm in order to have as a specification a value closer to the actual system results.

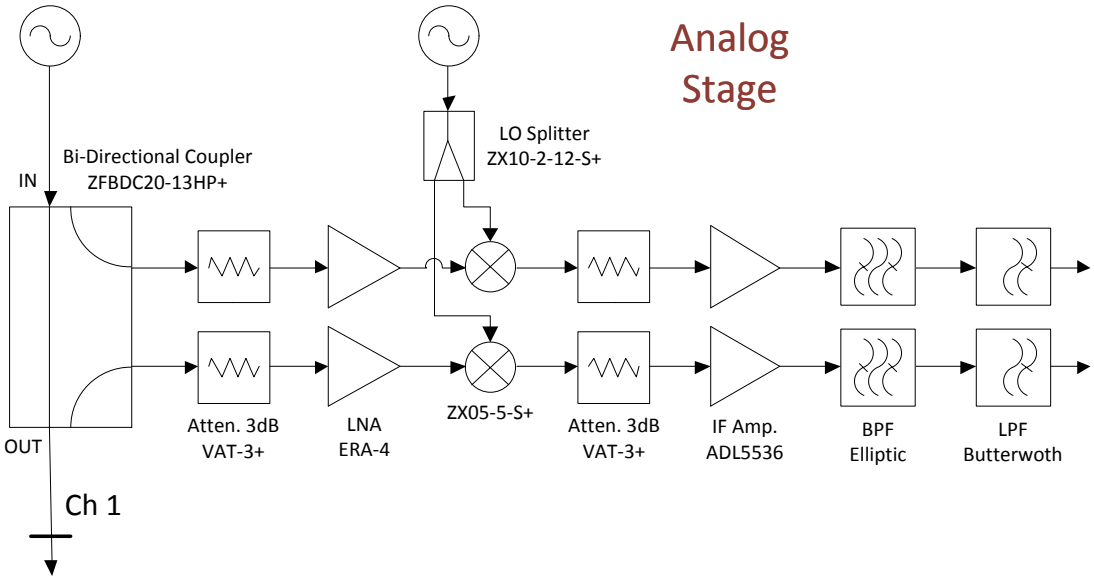


Figure 4.24: Final Analog Stage

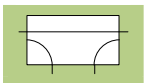
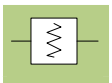
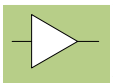
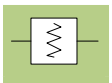
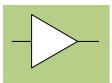
After this change the resultant IIP3 was now closer to the wanted value, but not yet in a secure value. So, a first attenuator was added to both paths. 3 dB attenuators from

Mini-Circuits, named VAT-3+ [31] was used. The 3 dB value is enough to put the IIP3 of the system on a safety number for the 5 dBm goal. Further this, after some simulations in ADS, was denoted that this attenuator improves the Incident Path Directivity in about 3 dB, also. High values attenuators don't increase the Directivity so, this was the value chose.

As the system still has a gain of 1,1 dB, which continues to be above the goal, an second change in the system was done for precaution. Due to the IF BPF, the return loss of the IF stage, outside the band pass region is in the worst case 3 dB. Which means that half the power that comes from the mixer outside the band pass frequency region will be back directly to the mixer. This lack of adaptation between the components can lead to a mixer malfunction. To prevent it from happening another two 3 dB attenuators was added to the system right after each mixer. This way, the RL of the IF sub-stage was improved by twice of the attenuator value, 6 dB.

The final analog system stage can be depicted on the figure 4.24. The calculations done in the worksheet for the final analog stage system were depicted in the table 4.2. The total gain of the system is now of -1,9 dB.

Table 4.2: Cascade Analysis - version 2

		 **Coupler**	 **1st Aten.**	 **RF Amp.**	 **Mixer**	 **2nd Aten.**	 **IF Amp.**	 **BPF**	 **LPF**
Component Values	Gain (dB)	-20,00	-3,00	14,20	-7,00	-3,00	20,10	-3,00	-0,20
	NF (dB)	20,00	3,00	4,20	7,00	3,00	2,40	3,00	0,20
	Input P1dB (dBm)	30,00	18,00	3,80	3,00	18,00	0,50	30,00	30,00
	Input IP3 (dBm)	42,00	30,00	20,80	15,00	30,00	20,90	42,00	42,00
Cumulative Results	Gain (dB)	-20,00	-23,00	-8,80	-15,80	-18,80	1,30	-1,70	**-1,90**
	NF (dB)	20,00	23,00	27,20	27,44	27,73	28,12	28,13	**28,13**
	Input P1dB (dBm)	30,00	29,36	24,88	11,59	11,57	10,89	10,82	**10,78**
	Input IP3 (dBm)	42,00	41,36	39,40	23,68	23,66	23,55	23,47	**23,42**

From the table an enormous value for the system NF can be denoted. This value isn't wrong, the NF is really this big. The reason for this result is the first chain component, the coupler, it attenuates the signal by 20 dB and so the NF after that can't be never below this 20 dB. As next to the coupler it was added another attenuator the NF is increased to 23 dB. However in this instrument the lowest input power level wasn't the big concern. When dealing with signals between -20 and 5 dBm, as the gain of the system is around -2 dB, the ADC full scale has to be set at least to 5 dBm. So, even with this enormous NF, the lowest test power that can be used in the instrument will not be limited by the NF value but by the noise floor of the adc.

As the analog stage is a translating frequency system, once again it cannot be characterized using the it's lab VNAs. So, to work around this problem the oscilloscope and some additional components was used in an arrange similar to what had been used on the Appendix A.

In the figure 4.25 can be seen the curve traces for the gain and isolation for both paths of the system. The predicted values for the gain are confirmed. In both paths, the variation from the initial gain value is about 2 dB. The isolation on the two paths is almost always greater than than 20 dB and after computing the Directivity, it is always better than 15 dB, which is a result that certainly will lead to a good measurement performance after adequate calibration. The gain difference of about 2 dB between the two paths doesn't have any immediate explanation, since the two paths were built with the same components and the coupler's coupling factor in the two paths is also similar, the two gain traces should coincide. However, the difference is not threatening, the calibration procedure will cancel it for sure.

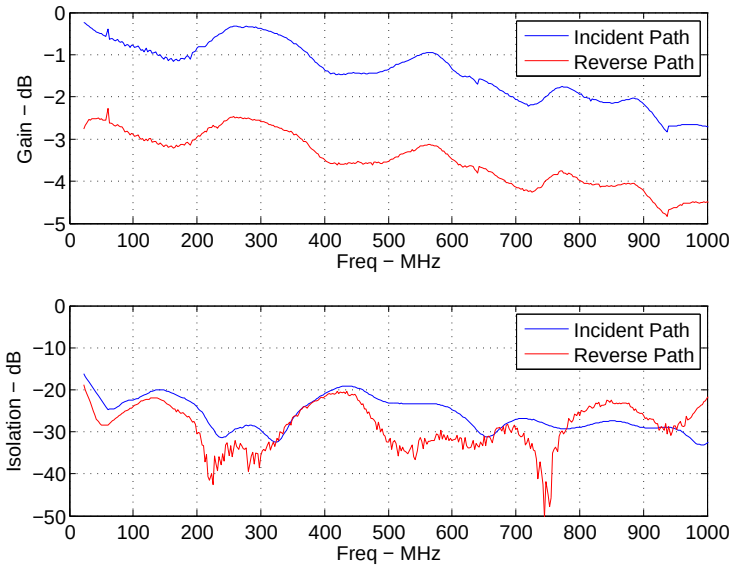


Figure 4.25: Final System Gain and Isolation, $P_{in} = -5$ dBm

The measured system P1dB can be depicted on figure 4.26. It was a little bit higher than what had been expected. From the trace, a 5 dBm input power value can be predicted as the upper limit to operate the instrument without measure distortion issues.

The results from the power sweep confirm the P1dB calculated and the maximum input power predicted. Even knowing that the initial goal has to be changed from 15 dBm to 5 dBm, this is not as bad as it sounds. Commercial VNAs had, after the coupler, a stepped attenuator, which produce a very high overall dynamic range. However, in a single measurement the dynamic range is much more limited due to the fixed position of the stepped attenuator during the same measurement, in order to avoid perturbations in the measure. If the 15 dBm goal for the proposed instrument was a crucial characteristic, it can be achieved by using an attenuator 10 dB higher in the place of the first attenuator. This way the maximum input power increases and the minimum input power decreases. The trade for this result was a loss in gain of 10 dB, also. So, to maintain the gain in the specified value, another amplifier will be needed in the end of the chain.

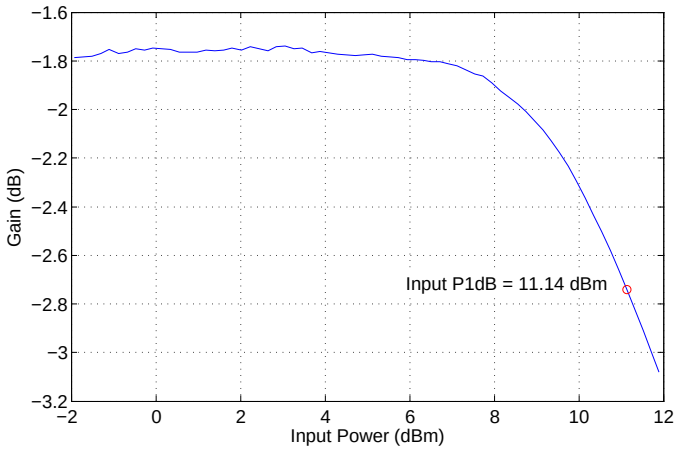


Figure 4.26: Final System Input P1dB, $f_{in} = 800\,\text{MHz}$

A photo of the built analog stage can be depicted on figure 4.27.

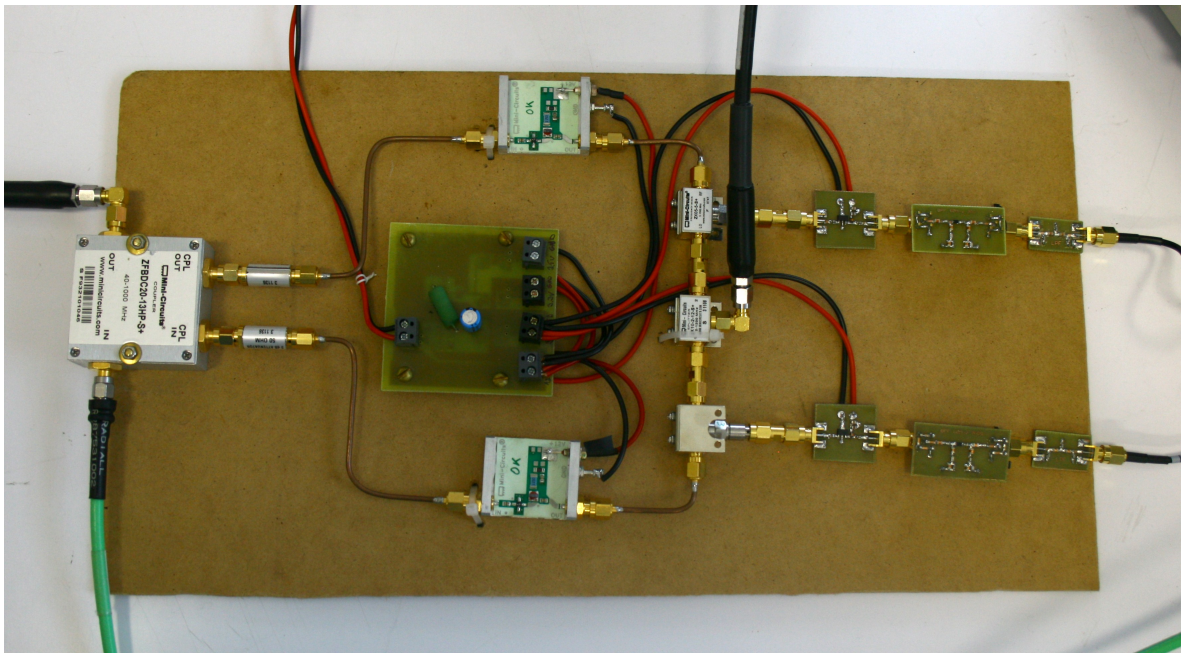


Figure 4.27: Photo of the Built Analog Stage

4.3 Digital Stage

To this stage of the system two blocks will be needed a two port ADC and a Digital Unit that can receive all the digital information from the previous ADC and together, serve as the Digital Front-End. This digital front-end has to be capable of receiving synchronous data from the DUT and generate digital signals to the DUT.

4.3.1 Digital Unit

The digital unit described has the same functions of a Logic Analyzer (LA). It should receive data in three channels synchronously, i.e. at the sample rate imposed by the component which is sending the data and not by its own clock. Two channels are occupied by the ADC that will be used to digitize the Analog Stage signals. The sample clock and the logic level used will be always the same in this case. However to read and send data to the DUT, the scenario is completely different. The major flexibility is achieved when multi logic levels at several sample rates could be received and sent, so it should be possible to read and send single-ended or differential signals with a flexible decision level.

To implement this block of the system the intention is to use a signal processor unit as a Digital Signal Processor (DSP) or an Field Programmable Gate Array (FPGA).

To achieve synchronous data reception the best option is the FPGA. The FPGA is reconfigurable hardware so, it could receive the clock signal from the ADC and make its receiving blocks work at the ADC sample rate. Contrary to the implementation using a DSP. Even thinking that a State-of-the-art DSP have a great processing power, with GHz speed and muti-core technology, it is not a good choice, because it works by its own clock and a polling or interrupt process must be do, in order to receive the data. However this data will be sampled only when the DSP clock allows it. Even considering the 80 MSPS sampling rate assumed for the intern ADC, which is 10 or so times less than the DSP clock, another operations besides the reception of data have to be done, the data received at some ports of the DSP has to be forwarded to a memory, in order to be treated later. To do all this steps a very caution programming must be done and even so, problems aren't impossible to happen.

With the use of an FPGA the clock sent by the ADC will be the clock used to receive all the sampled bits. Furthermore, in modern FPGAs already exist carefully designed clock distribution schemes, like the one on figure 4.28 and clock control mechanisms, like Digital Clock Manager (DCM)[32], that take care of the signal and feed all the blocks selected to use that signal without delay between them or even delay between the input signal clock and the signal that reach each one of the blocks. These very powerful mechanisms are the right choice to perform synchronous reading from the ADC.

Old development boards designed to receive data from ADCs used First In, First Out (FIFO) memories. The FIFO memory has the advantage of being capable to receive synchronous data. Besides, it is a low cost alternative and it is very easy to use. On the other side, the FIFO memory is a much more limiting implementation, the data bits much reach it in parallel, it couldn't accept data from ADCs with serial outputs, as the case of Texas Instruments (TI) ADS6225. Instead, the FPGA could be programmed to receive serial data, if its maximum working frequency allows it. The FIFO by itself only could take the sampled signal and store it. To use the data, an additional processor unit has to be used. In this case, a DSP or even a general propose processor could be used, because the intention is to perform the demanding calculations on a Personal Computer (PC). In contrast to the FIFO, where

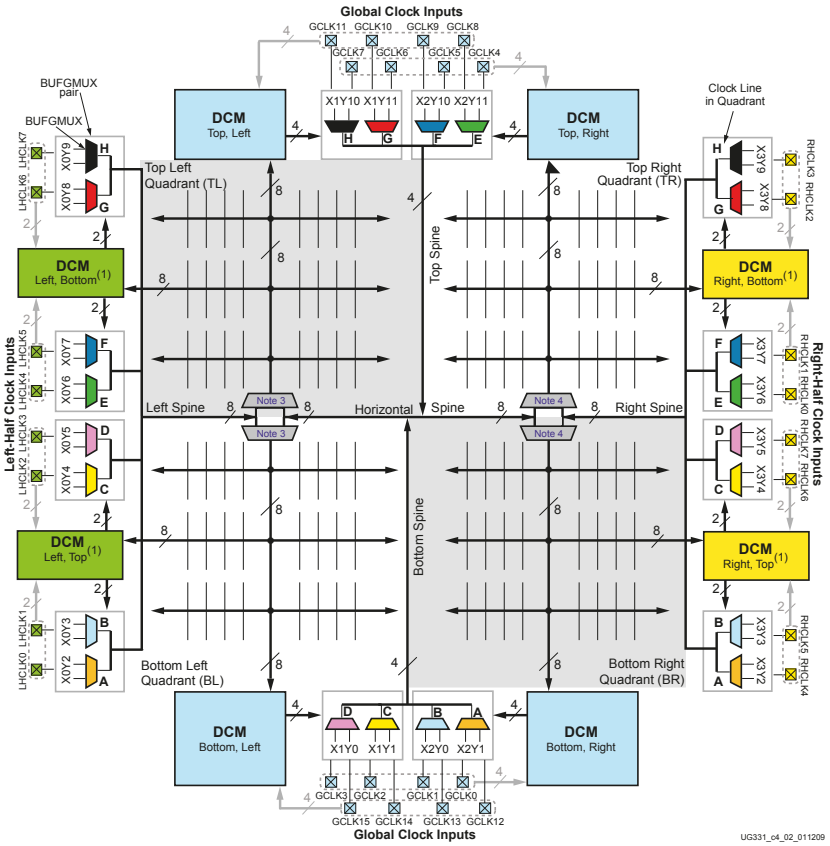


Figure 4.28: Quadrant-Clock Distribution of Xilinx Spartan 3 FPGA, from [3]

the data much reach it in parallel.

Considering the generation of digital signals, the FPGA remains as the only alternative. To do this task it is the only component mentioned until now, that could generate user defined signals at different rates. So it is the only signal processor capable of performing well all the desired tasks.

Although the good advantages of the FPGA, they exhibits a high learning curve. The adaptation to its development tools, which means an adaptation to VHSIC Hardware Description Language (VHDL) or Verilog, in order to program the FPGA can be very time consuming. The addiction of an FPGA development certainly will exceed the reasonably dimensions of the entire project.

Therefore, in the ideal scenario, use an FPGA to do this job is also a very difficult task. Because commonly FPGAs as the other signal processors are designed to interface with a specific logic level.

Due to the previous reasons and due to the high cost of an FPGA development board, it was decided to use a Logic Analyzer as the Digital Unit to receive all the data from the ADCs and to generate the stimulus digital signal using its Pattern Generator function.

4.3.2 ADC

As assumed on section 4.2.4, the ADC to be used should has an maximum sampling frequency grater or equal to 80 MSPS. Once there are two paths to digitize, a 2 analog channels ADC must be chosen, in order to digitize the two paths at the same time so, this way it is possible to compare the two digital signals directly.

At the IT's stock already exist the evaluation board of the TI ADS6225, previously mentioned. It is an Dual 125 MSPS ADC with Serial LVDS outputs [33], it is exactly what has needed to the project. After the analysis of the evaluation board datasheet [34], it was noticed that the digital output connector is a Samtec QSH series, that mates with a Samtec QTH series presented on the TI analysis board to them evaluation boards, the TSW1200 [35]. As this Samtec connector is an expensive and hard to solder component, the adaptation to the LA probes was not possible. Besides, an adapter was not found so, the use of this evaluation board has to be left behind.

After a several search for an ADC evaluation board that fulfil the requirements and has an direct connection to the LA 40-pin cable (40-pin header 2,54 mm), it was found the MAXIM MAX1259ETK[36], an evaluation board of the MAXIM MAX1259 ADC, this was an 96 MSPS, 14 bits ADC. But it was not available to buy anywhere and any other board was, at least at a reasonable price. So, it was decided to design and produce a board, in order to reduce costs and to provide for a direct connection to the LA.

The chosen ADC was the MAX1180 from MAXIM, and its features are [37]:

- Dual channel
- 10 Bits per channel
- 105 MSPS
- Parallel Outputs
- 48 Pin TQFP Package

The 10 bits ADC has an ideal Signal-to-Noise And Distortion ratio (SINAD) of 61,96 dB. The values on the datasheet gave a better idea of the ADC real performance. For a test signal with $f_{in} = 50,078$ MHz and $P_{in} = -0.5$ dBFS at $f_S = 105,263$ MHz, the following values can be found:

- SINAD – 58 dBc
- SFDR – 70 dBc

With the SINAD referred, 9,3 Effective Number Of Bits (ENOB) can be calculated, which is a satisfactory value. In the end the 70 dBc SFDR ensures good results in a wide dynamic range.

Building the board

The basis design to build the board was the MAX1180 Evaluation Kit itself[38]. From there it was possible to check what were the suitable components to build around the ADC IC in order to provide in the board all its functional parts. With this information and with the information contained on the IC datasheet, it was possible to choose the list of components to complete the board besides the IC, the main ones are displayed next:

- Single-ended to Differential Conversion – Coilcraft WB1-1TSLB.
  In order to convert the two input IF signals to differential signals needed at the ADC's inputs, two of this transformer were used, they work inside the IF bandwidth with a low insertion loss.

- Clock Driver – MAX9113[39].
  It is a dual low pulse skew differential to single ended driver. It allows the conversion of a differential sinusoidal signal into two squared single ended clock signals that are needed to be used as clock inputs of the ADC and digital output driver ICs. To feed the MAX9113 with the differential signal needed, it was used the Coilcraft WB4-1HSLB, another transformer as the ones used to the IF input signal.

- Digital Output Drivers – TI SN74AVC16244[40]
  Two output drivers was needed to drive out the ADC digital outputs. Those ICs are non-inverting CMOS drivers, that work with the levels and at the frequency required.

From the evaluation kit datasheet, once again, and from several high frequency design guides it was possible to get some help to understand the principal concerns in design such a complex board as an ADC evaluation board. The length of all the input signal lines had to be the same and the same rule had to be applied to the output digital lines before the IC driver, to the output digital lines after the driver and to the clock lines. The ground vias should be placed as close as possible to the ground pins and should be one per ground pin. Due to the noise produced by the digital components the two grounds should be physical separated. Finally all the source points must be properly decoupled with capacitors.

To have a reasonable RL an abortive load had to be placed to match the ADC input ports with a very high impedance to 50 Ω. Before the final board could be produced, an intermediate step was taken in order to evaluate the transformer performance and assure its ability to receive the IF signal, by measuring its Insertion Loss and Return Loss. After good results had been achieved the total board could be designed.

The final board's schematic and PCB layout are shown on C.4.1.

Results

In first place the input impedance of the two ports was measured. Good results were achieved, with a return loss before 70 MHz better than 15 dB as can be seen on figure 4.29b. The smith chart of the same measurement can also be seen on figure 4.29a.

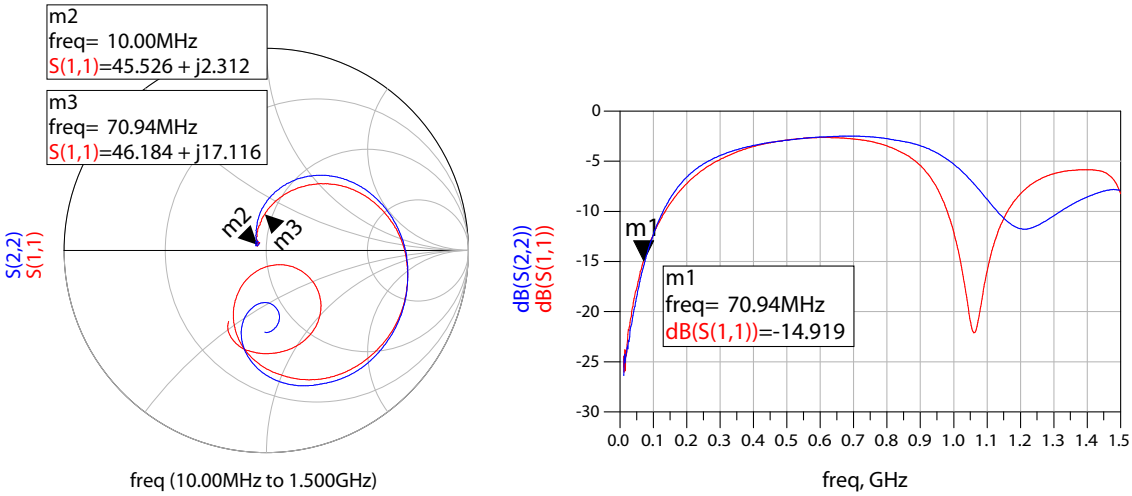
To connect the Digital Outputs to the LA a probing circuitry was needed. To avoid the general purpose, flying lead probes, an isolation circuit was design. It is depicted on C.4.2.

In the first time connection of the board, the bad news appeared. One of the ADCs channel is not working at all, some of the bits are always in the same state instead of changing their state due to the input signal. This problem is probably due to some line breaks in the output lines of the ADC. However, at least the another channel seems to be working.

In figures 4.30 and 4.31, some test results could be seen.

As can be seen in the figure 4.32 the results with flying lead probes and with the isolation circuit are closely similar so all indicates to its good functioning.

The clock signal that fed the ADC IC was measured and it result is depicted in figure 4.33.



(a) Smith Chart (b) Return Loss

Figure 4.29: Input Impedance of the two ADC ports

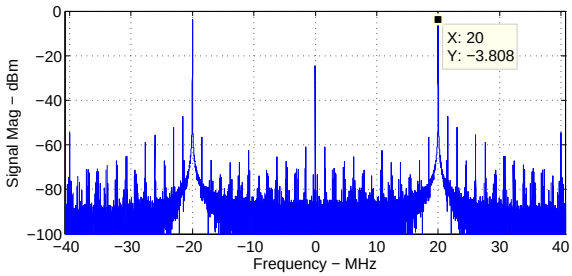
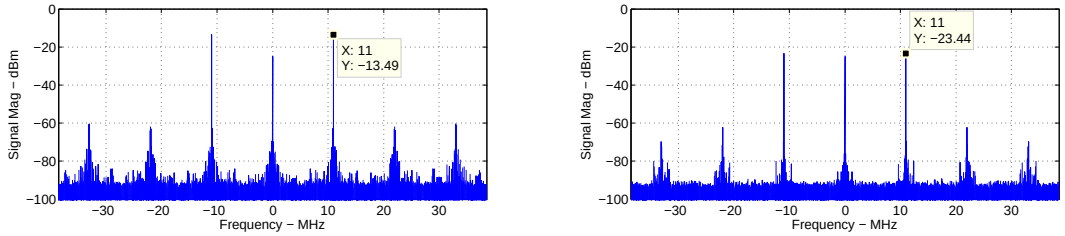


Figure 4.30: ADC result for a 1-tone, 20 MHz, 0 dBm signal, with $f_S = 81,527$ MSPS



(a) -10 dBm input signal (b) -20 dBm input signal

Figure 4.31: ADC result for a 1-tone, 11 MHz input signal, with $f_S = 77,1$ MSPS

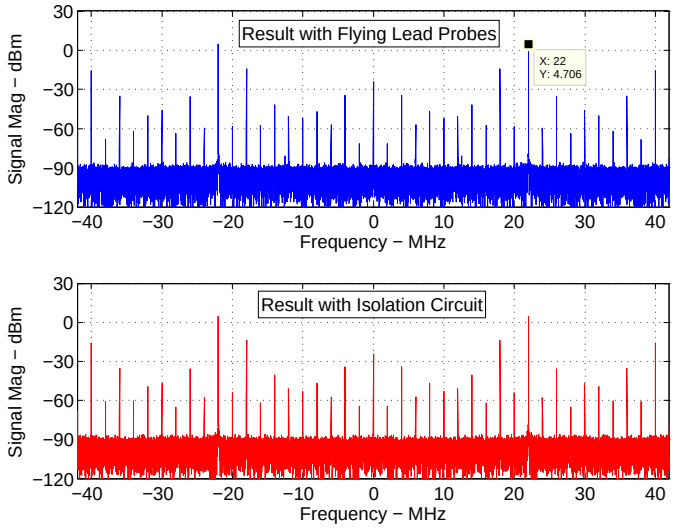


Figure 4.32: ADC result for a 1-tone, 22 MHz, 10 dBm input signal, with $f_S = 84$ MSPS

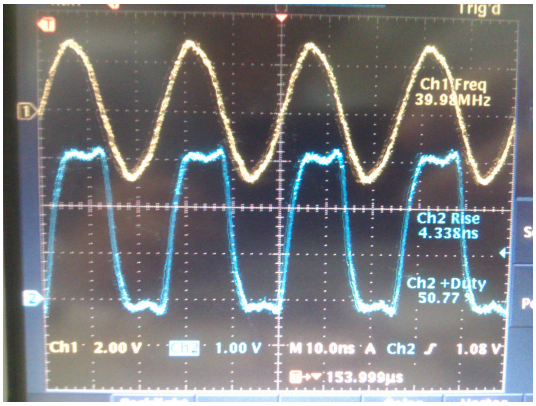


Figure 4.33: ADC clock signal measure, input signal with 40 MHz and 10 dBm

4.4 Signal Generators

Several signals must be generated to feed the various blocks of the system. In sake of simplicity lab generators were used to do the work. The local oscillator signal is an one-tone sinusoidal signal and to generate it was used the HP E4433B - ESG-D [41]. The ADC clock source is also an one-tone sinusoidal signal and to produce this one, was used the Rohde & Schwarz (R&S) SMR40 [42].

The main stimulus signal could be a simple one-tone signal, but can also be a multi-tone complex signal. Thus to generate such signals, the R&S SMU-200A [43] was used. It has an internal 100 MHz DAC, which can be used to convert to the analog domain signals produced in a software such as the MATLAB®. To do it and to remotely control the remain instruments, it was used the procedure explained in the next section.

4.5 Lab Equipment Communication

To complement our implementation in order to have a complete analyser is necessary to interact with signal generators, with the Logic Analyser and the Oscilloscope. The goal is to fully control all the instruments from a main software, a MATLAB®routine that control the measure flow and proceed with the necessary calculations.

To interact with these several equipments within, the MATLAB®environment Standard Commands for Programmable Instruments (SCPI) commands were used. The SCPI standard defines a set of commands, that are American Standard Code for Information Interchange (ASCII) textual strings. These commands are intended to use in the control of measurement instruments from different manufacturers. Two types of commands could be defined:

- **Setting commands** – Used to define instrument settings, e.g. "`*WAI`" will set the instrument to prevents from executing further commands until all pending operations finish, and "`HORizontal:MODE:SAMPLERate 625MHz`" will set the sample rate of the instrument.

- **Queries** – Used to subsequently receive data from the equipment, e.g. "`CURVe?`" will make the instrument transfer the waveform acquired data.

Some commands could be at once a Setting and a Query command. The error handling is performed using queries to verify the instrument status.

However this commands intend to be universal, each one of the instruments has different text forms to use them. This happens due to the different functions available in different instruments or just due to manufacturer policy. To found the specific wanted commands, the author search in the correspondent instrument manuals, or programmer manuals, [42], [43], [44], [45]. All the examples presented before are commands to control the Oscilloscope used, the Real Time Tektronix DPO72004B.

As the SCPI standard don't define the interface level, post drivers will be needed to configure the physical connections between the PC and the instruments. In order to unify the interfaces, an universal Input/Output (I/O) library was created by several Test and Measurement (T&M) companies, the Virtual Instrument Software Architecture (VISA) Library Maintained by the Interchangeable Virtual Instrument (IVI) Foundation. It intends to be independent of the physical layer and largely assures it.

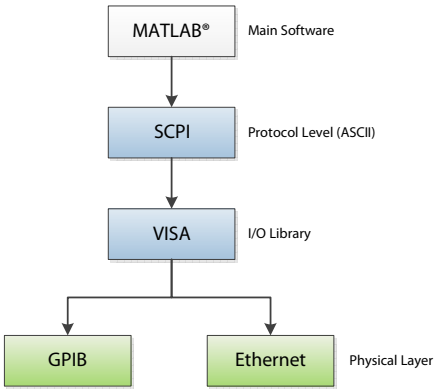


Figure 4.34: Remote Control Flow Chart

To connect the PC and the necessary instruments two interfaces were used. The Local Area Network (LAN) - Ethernet was used whenever it was available in the equipment, otherwise it was used the General Purpose Interface Bus (GPIB) over an USB adaptor. The VISA library was used to assure portability between interfaces.

A design flow of the control structure is shown on the figure 4.34.

The LA used, the Agilent 16822A, doesn't have available remote control through SCPI, it has only available Distributed Component Object Model (DCOM) remote programming. Due to the late discovery of this limitation and to the lack of experience in DCOM, a communication with the LA was not achieved. So, with this instrument only a trigger signal and a pre-loaded configuration were used to take sequential measurements.

4.6 Power Source

To feed all of the hardware a power source will be needed. To do that, the power that each component consumes has to be known. Thus, each component has the following needs:

- LNA - 12 V at 65 mA each;
- IF Amp. - 5 V at 109 mA each;
- ADC - 2,5 V at 100 mA and 3,3 V at 300 mA.

The values presented before to the ADC are the recommended ones on the Evaluation Kit from Maxim[38] (guide line to construct the assembled ADC board). The values presented seemed to be reasonable, once the ADC IC itself consumes from the 3,3 V source 125 mA and on the board there still the clock driver IC and the two digital output drivers.

In order to reduce the complexity of the power source board, a laboratory power supply will be used to provide for the stabilized 12 V. From this main source a switching IC regulator will produce an intermediate lower voltage. Then, several Low-Dropout Regulator (LDO) linear regulators will transform this voltage in each one of the required output voltages.

For the 2,5 and 3,3 V an additional LDO was put between it and the switching regulator, to attenuate even more the switching noise and to surpass the even high voltage drop between the switching regulator output and the wanted outputs.

The ICs chosen and their characteristics are shown on table 4.3. Three different LT1763 were used to produce the wanted output voltages. To have the 2,5 V output was been used the LT1763-2.5, to 3,3 V the LT1763-3.3 and to 5 V the LT1763-5.

IC	TPS5420	LT3080	LT1763
IC Vendor	Texas Inst.	Linear Tech.	Linear Tech.
Regulator Type	Switched	LDO	LDO
Max. Output Current	2 A	1,1 A	500 mA
Typ. Dropout Voltage	–	1,2 V [a]	300 mV
Switching Frequency	500 kHz	–	–

[a] To the package used. For other packages the LT3080 has a dropout voltage of 350 mV.

Table 4.3: Regulators chosen and their characteristics

Besides the regulators, the other board components are calculated and chosen from each one of the ICs datasheets, [46], [47] and [48]. The entire board schematic are depicted on C.15, and its PCB are also depicted on C.16.

4.7 Final System Arrangement

The impossibility to remotely controls the Logic Analyzer, allied to the ADC malfunction, where only one channel is working, remains as the two barriers in the total execution of the proposed work. Once, the source of the ADC malfunctioning could be very hard and time consuming to find and because no solution appears in sight to overcome the Logic Analyzer communication problem, the measurement procedure will be slow and less than automatic.

So, even with advantage of an high dynamic range if an ADC was used, the decision was to put the ADC aside and use the oscilloscope to digitize the incident and reflected signals at the end of the respective paths. This way, at least to measure analog components a fully automatic and relatively fast instrument could be realized.

The final system arrangement with the LA and the oscilloscope is shown in figure 4.36, a photo of the built analog stage connected to the oscilloscope can be depicted on figure 4.35.

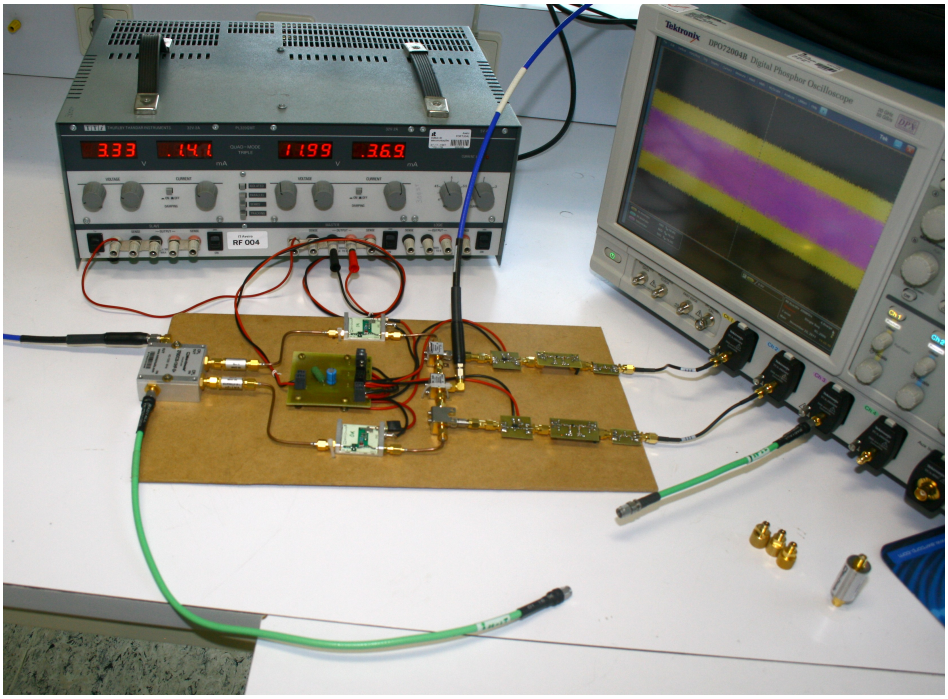


Figure 4.35: Photo of the Instrument built, ready to characterize an analog component

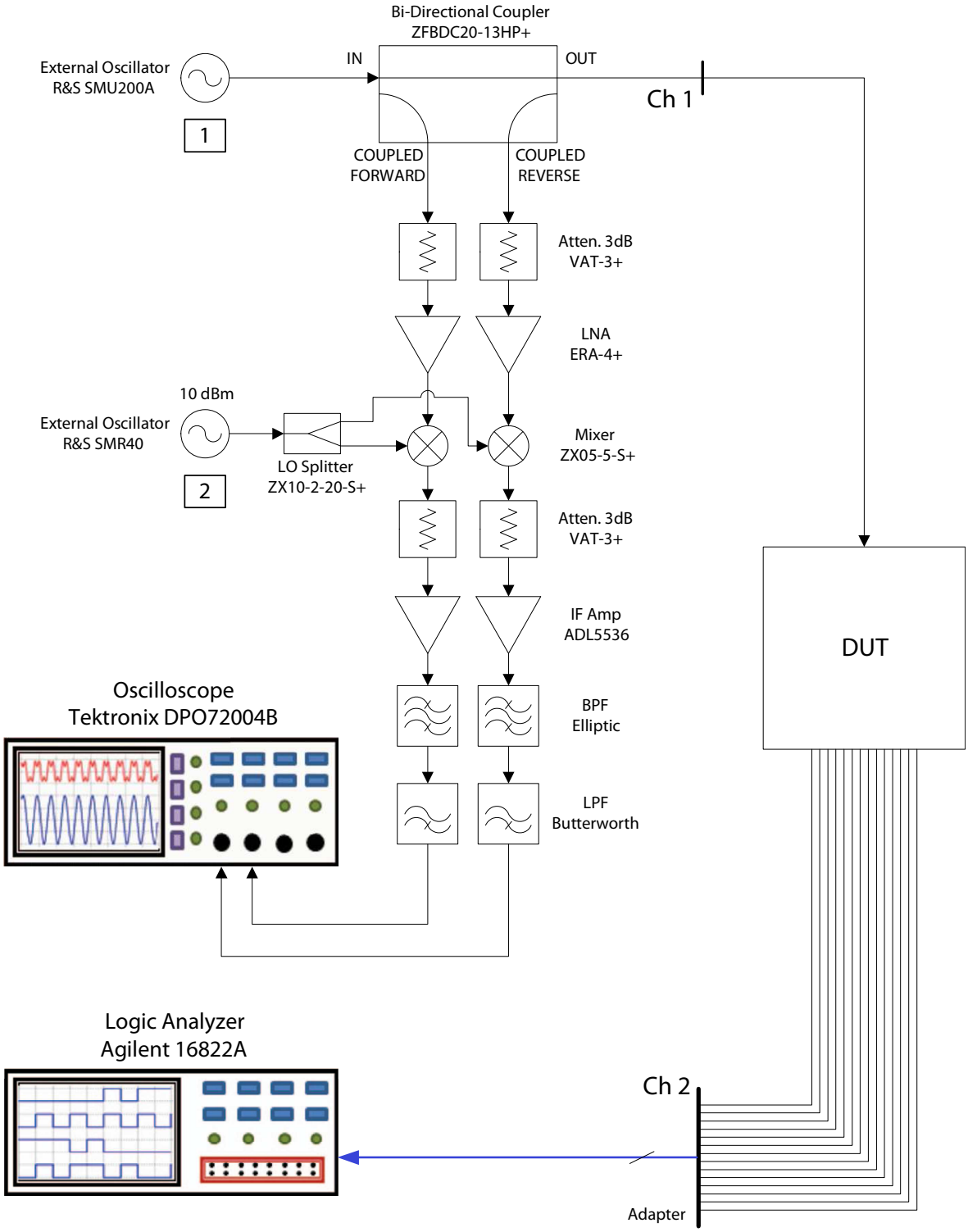


Figure 4.36: Final System with Oscilloscope

Chapter 5

Taking Measurements

In the instrument presented only frequency sweep measurements were carefully implemented, calibrated and tested. Although the instruments has the characteristics to proceed a power measurement, additional calibration is needed to obtain meaning values.

5.1 Reflection Coefficient

The reflection coefficient of the DUT can be measured in the same way it is measured on traditional VNAs. The incident and the reflected signals received at the end of the Reflected and Incident paths could be directly compared each other, however a calibration process to eliminate some mismatches is mandatory. Then, the true value to reflection coefficient is found.

The calibration process will be explained in the section 5.4.

5.2 Gain

To build the proposed instrument, was adopted a traditional VNA architecture front-end to the analog port and an LA like front-end to the digital port.

To measure the gain phase relation from the input to the output of the DUT is mandatory to have a synchronous and unaffected in phase reading from both the ports of the equipment, in order to compare the phase of input and output signals. Traditional VNAs has a super-heterodyne architecture front-end in all the ports, as shown on figure 3.3, which means it doesn't introduce phase impairments in the measure because all the signals are down-converted by the same LO, and so the phase error, due to the LO phase on down-conversion, are cancelled each other, as expressed on equation 3.2.4 that was written again here, on equation 5.2

$$\phi_3 - \phi_1 = (\phi_{OUT_3} + \phi_{LO}) - (\phi_{IN_1} + \phi_{LO}) \iff \phi_3 - \phi_1 = \phi_{OUT_3} - \phi_{IN_1}$$

In the proposed configuration this is quite different. Due to the mixed-domain nature of the measurement, it is impossible to affect the digital signal with the same LO used to down-convert the analog signal. As the down-conversion on the analog path is used to put the RF stimulus signal of the DUT on a IF frequency readable by the analyzer converter, the LO signal will be near to the RF frequency in order to have a low IF. Thus the digitization of the LO is already discarded because it will be as difficult as digitize the RF signal.

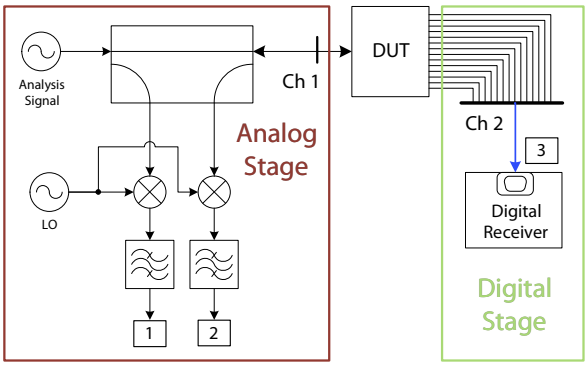


Figure 5.1: Simplified block diagram of the proposed instrument

To surpass the phase impairment issue, another measure technique has to be explored. The technique presented here uses an excitation signal with two tones, as recently presented by R&S [49], to characterize the phase response of a mixer without access to its LO. So the great advantage of this technique is its immunity to the LO phase. This is exactly what is needed to perform phase related measures on the mixed-domain proposed instrument.

5.2.1 The Two-Tone Technique

The basis of this technique is the use of a two-tone signal to excite the DUT. Measuring the phase difference between tones at the input of the DUT and measuring again this difference at the output of the DUT, it is possible to know the phase delay imposed by the DUT from one frequency to the other.

In the figure 5.2, the tone at f_A of the incident signal has ϕ_a phase and the tone at f_B has ϕ_b phase, the measured incident signal represented by **1** on figure 5.1 will have f_C with ϕ_c phase and f_D with ϕ_d phase in figure 5.2. Considering only the mixer contribution to the phase delay on the front-end incident path, the measure of the incident signal, can be expressed by the following expression:

$$\phi_1 = (\phi_a + \phi_{LO}) - (\phi_b + \phi_{LO}) \iff \phi_1 = \phi_a - \phi_b = \phi_{INC} \tag{5.1}$$

So the relation between the tones of the measured incident signal is exactly the same as the incident signal itself. Thus, with this approach the phase error introduced by the LO on the analog down-conversion section is canceled and the results will be immune to the LO phase.

The phase relation obtained is only the phase delay from one frequency to the other, this means it is a relative phase measurement. So, if the goal is to have the phase response of the DUT across the frequency, each measurement must be added to the previous one in order to produce the wanted trace. The result must be the equal to the one taken by the traditional one tone technique[1] except for an offset value, that corresponds to the phase delay of the first frequency of the sweep that for simplicity could be considered as zero.

Although, it was not possible to have the absolute phase delay of the DUT for a specific frequency, the important thing in communications is to know that the phase is linear along

[1]Considering conditions where the one-tone technique is valid, like when using a glsvna to measure an all analog DUT without frequency conversion blocks

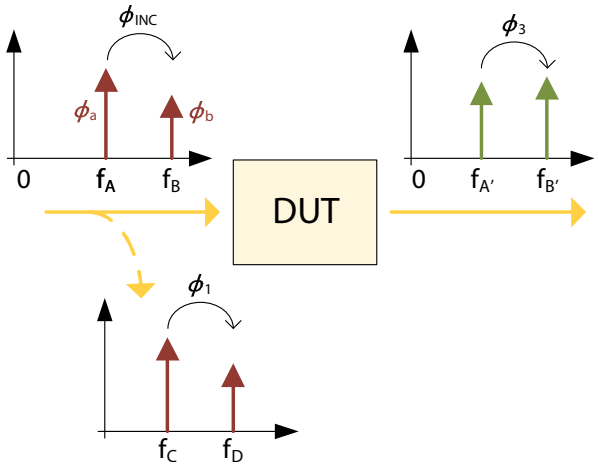


Figure 5.2: Illustration of the signals on the 2-tone technique

all the bandwidth where the transmitted signal is placed in order to avoid distortion on that signal. Thus, the relative measurements should be enough to ensure the correct functioning of the SDR.

So, the two-tone technique has crucial advantages over the one-tone procedure traditionally used on VNAs, which makes its study and analysis important to achieve the goal of construct a Mixed-Domain Instrument that could characterize quickly and easily an SDR.

In a Network Analysis system there is the need to ensure that both samples of the signals to be compared have been taken at precisely the same time, if this wasn't accomplished the results will suffer from errors, principally the phase results. This can be easily understand due to the signal phase definition, its value will depend on the instant that the sampled signal began to be acquired. If the two signals, the incident and the transmitted, began to be acquired at different times the comparison between the two most certainly don't result in the real phase response of the DUT. This issue will be increased by the growth in the signal frequency, because the phase of the signal with a higher frequency will rotate more quickly.

Here, the two-tone technique is an added value to the measurement because the time of a full phase rotation between the two tones will be dictated by the space frequency between those tones. Thus, if the frequency separation has been set low enough, the uncertainty time in the synchronization of the triggers will lead to a phase error that can be ignored.

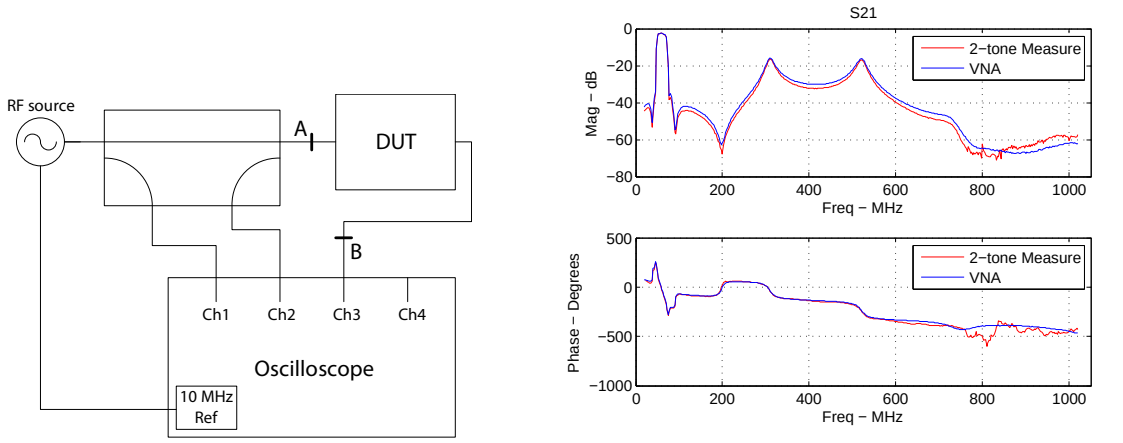
Measurement Procedure

As seen on figure 5.2 the two tones do not have the same power, the second is below the first. This was the procedure followed, and so the second tone used to stimulate the DUT on the laboratory implementation of the technique, has less 10 dB than the first one, in order to reduce the Peak-to-Average Power Ratio (PAPR) by reducing the influence of the second tone on the peak and average power available at the input of the DUT.

In order to compute the phase trace result, each step point relative phase have to be added to the previous ones, which means a cumulative sum have to be performed. The first frequency point is assumed to have 0°, as said before and from then on, the relative phase will be added consecutively. The negative part of this implementation is its vulnerability to propagation errors from one step to the next.

Format Validation

To validate the ability to perform accurate measures of both magnitude and phase gain, a simple test was done. The lab arrangement can be depicted on figure 5.3. In the measurement no down-conversion exists and a single tone measurement could be taken, however the intention is only to watch the ability to take magnitude and phase gain measurements with the 2-tone technique in the most simple case.



(a) Lab Arrangement

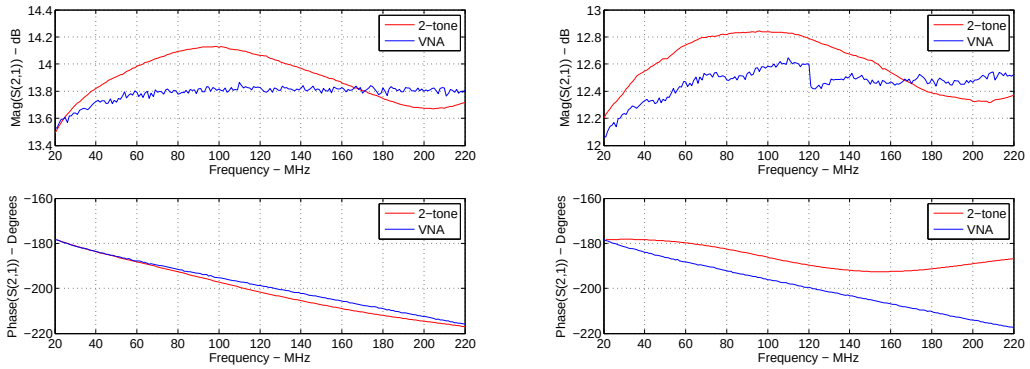
(b) IF BPF frequency response – 20 to 1020 MHz

Figure 5.3: 2-tone Test Measure Lab Arrangement and BPF response

The figure 5.3b reveals the test of the IF Filter implemented on section 4.2.4. The results were very good, both magnitude and phase have a well match. This measurement was done from 20 to 1020 MHz with 2,5 MHz space between tones.

In the figure 5.4 are depicted results for the Mini-Circuits ERA-4 Amplifier used on section 4.2.2. As said before, the 2-tone measurements were performed with the second tone 10 dB lower than the first, resulting in a PAPR of 5 dB, 2 dB higher than the PAPR of a single tone signal. In the figure 5.4a the amplifier was measured in its linear region, on the VNA was used 0 dBm input power and on the 2-tone measurement the higher tone has -3 dBm. In the figure 5.4b the amplifier was measured in its non-linear region, on the VNA was used 5 dBm input power and on the 2-tone 2 dBm for the higher tone. Both measurements were done from 20 to 220 MHz with 1 MHz space between tones.

When the amplifier was operated in the linear region, the results are according with the results from the VNA. But, when the amplifier was operated in its non-linear region the phase gain result was not so accurate. In non-linear operating conditions, intermodulation will occur so, the phase of each tone will be affected by the intermodulation products, which with a two tones signal are different from the case with only one-tone. In this condition, the phase results from the 2-tone measurement won't follow the results from the VNA at all. In conclusion, is not possible to take VNA-matched results with the 2-tone technique if the DUT was measured in its nonlinear region of operation.



(a) ERA-4 frequency response at 0dBm

(b) ERA-4 frequency response at 5dBm

Figure 5.4: 2-tone ERA-4 Frequency response comparison, from 20 to 220 MHz

5.3 Global Procedures

The complex proprieties of each frequency point value must be known in order to calculate the reflection coefficient and the gain values for a frequency sweep measurement. Thus, to calculate the magnitude and phase of a specific frequency, a MATLAB®algorithm was developed based on the Fast Fourier Transform (FFT) of the signal. Firstly, in order to match the frequency of the stimulus signal with only one point of the FFT, the total number of points to compute the FFT is determined for each one of the tones, taking into account the frequency of the stimulus signal and the sampling frequency used. After the FFT had been obtained the Fourier coefficients completely define in phase and amplitude its corresponding frequencies.

An alternative implementation, which probably is the most common on commercial VNAs, is the use of an In Phase/Quadrature (I/Q) Demodulator Receiver. Actually, it is implemented in the Digital Domain, in order to reduce costs and maximize flexibility. An illustration of the architecture is depicted in the figure 5.5.

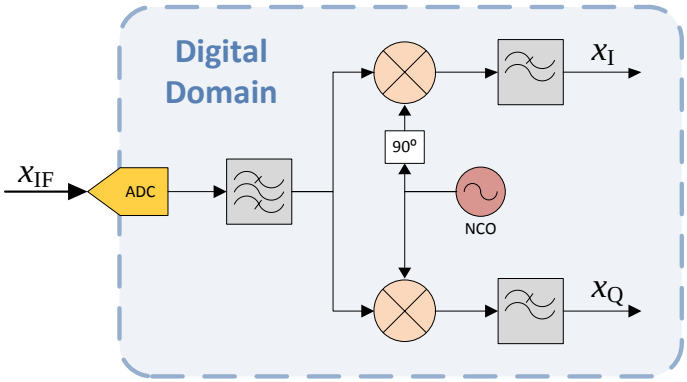


Figure 5.5: Digital Detector using an I/Q receiver

The input of the system is a digitized version of the IF signal. In the end of the architecture the phasor that describes x_{IF} at frequency $f(NCO)$ is given by the DC signals x_I and x_Q, x_I

gives the real part, while x_Q gives the imaginary part. This way the complex FFT algorithm is avoid and the number of samples are uncorrelated with the measure bandwidth, since the final measurement bandwidth[2] depends only on the bandwidth of the last LPF. The number of samples and the sampling frequency are independently of the measured frequency, also. A unique sampling frequency could be chose and if it is uncorrelated with all the frequencies in the IF bandwidth, is possible to know the real and imaginary characteristics without being limited by the FFT frequency resolution.

In the actual implementation, it was decided to use the FFT, due to its direct method to obtain the wanted results. In the FFT, the number of samples used to perform it, defines its frequency resolution, which is the bandwidth used to calculate each of the FFT coefficient. This way, taking a large amount of samples for each measurement point gives directly a very straight measurement bandwidth, without further processing. However, the I/Q demodulator process could be implemented to run much faster than the FFT process, but in this project the processing time wasn't a main goal.

With the information of a specific frequency, the remain process is only calculate the ration of the complex values between the right frequencies. As presented in section 5.2, to compute the phase gain, the phase between the two tones at different frequencies must be calculated. With the FFT process, this is an easy task. So, if care had been taken and the value for the two wanted frequencies is represented completely in the same FFT, to obtain the wanted phase relation, the two complex values only has to be related.

5.4 Calibration

Every measurement performed by any kind of instrument has within it an amount of uncertainty. This uncertainty is the result of several errors occurred during the measurement procedure. These errors could be **Random Errors** or **Systematic Errors**.

Random Errors – despite they could be statistically described, they are impossible to correct using systematic methods. If the random errors have impact on the measurement, poor repeatability will be observed, i.e. variation in the results occurred in the same measurements with the same conditions. Several sources of Random Errors are present in every measurement and should be kept as low as possible. The Thermal Drift is a random error, it is also known as **Drift Error** and to avoid it an instrument warm-up should always be done, so the temperature should be constant during measurements.

Systematic Errors – this kind of errors are repeatable over time and temperature. Therefore they can be characterized and then corrected using calibration methods, over the assumption they are time invariant. Over the years, several calibration procedures were developed to VNAs.

Even the finest instrument have imperfections, which lead to less than ideal measurement results. The Systematic Errors are due to imperfections in the analyzer. One of the major

[2]The measurement bandwidth is the final bandwidth used to perform the complex phasor calculation. Like on receivers, the bandwidth is related with the total amount of noise received. The amount of noise will limit the minimum signal power level in which the instrument is still able to perform measurements.
In the case of a VNA, the goal is to know the complex value of the sinusoidal signal phasor so, the ideal value for the bandwidth will be 1 Hz. However a very straight measurement bandwidth usually leads to high processing time and so, typically values of 10 kHz and 1 kHz are used in commercial VNAs. Nevertheless this is an option that could be defined in the VNA menu.
Improvements using averaging techniques are also employed, in [50] this topic is discussed more deeply.

source of this errors is caused by the directivity of the directional component. The non-ideal characteristics of this component leads to some leakage and so, some of the incident signal will appear in the reflected path and vice-versa. In the figure 5.6 is represented the signal flow when the intention is to measure only the reflected signal, as can be seen some of the incident power leaks into the wrong path and joins the real reflected signal. Thus the measured quantity will be the sum or the subtraction of the two, depending on their phase. When the DUT has a good adaptation with the system Z_0, the reflected signal will be very low and the leakage power may be as high as it. In this situation, without calibration, significant measurement errors will occur.

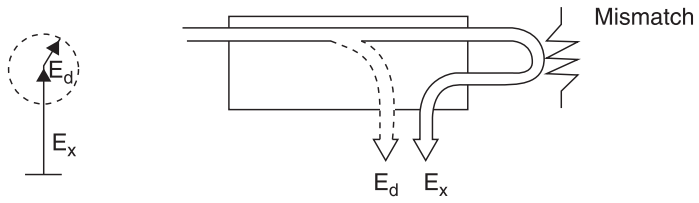


Figure 5.6: Return Loss error due to directional component directivity, from [4]

The Calibration Reference Plane is one important definition when someone is performing a calibration in a VNA. It sets the physical location at where, after the calibration procedure, the DUT begins. The final trace result will be affected by everything, from there on. When coaxial measurements were performed, with a previous suitable calibration, the Reference Plane will be at the matting plane of the outer conductor, as represented on figure 5.7 for PC3.5, 2.4 mm and 1.85 mm connectors.

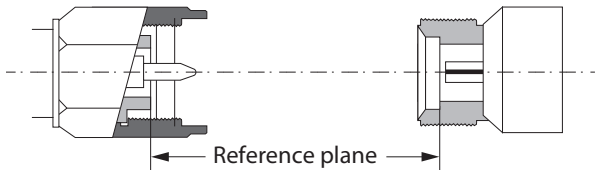


Figure 5.7: Reference Planes in Coaxial PC3.5, 2.4 mm and 1.85 mm connectors, from [5]

To measure and calculate the error parameters several methods could be used. The most common is based on known SOLT (Short, Open, Load, Thru) termination standards. To each standard a model was developed, based on the physical characteristics of each standard. Thus, using a series of parameters an accurate frequency response could be calculated to the wanted frequency span.From [51] it was possible to understand the definitions for each one of the standards used. Then, the following definitions were used:

- Open – The Open is modeled as an impedance Z_O, defined by:

$$Z_O = \frac{1}{j2\pi f C_O}, \text{ with } \quad C_O = C_0 + C_1 f + C_2 f^2 + C_3 f^3 \tag{5.2}$$

  Besides, it has also a delay introduced by the transmission line from the reference plane to the actual position of the open, as shown on figure 5.8a.

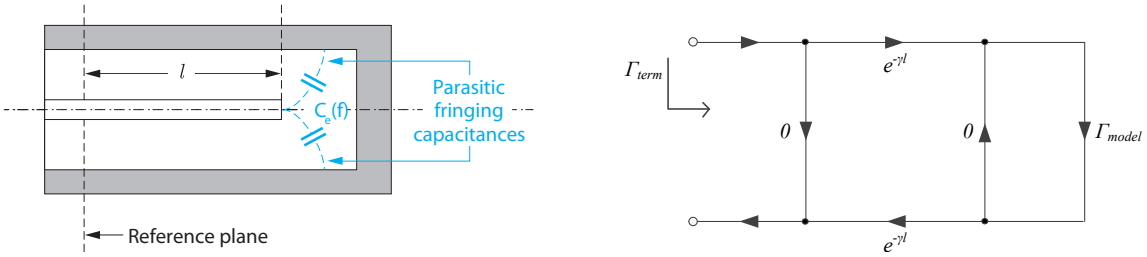
- Short – The Short is considered in old VNAs as an ideal short. However in modern VNAs it is modeled as an impedance Z_S, defined by:

$$Z_S = j2\pi f L_S\,, \text{ with } \quad L_S = L_0 + L_1 f + L_2 f^2 + L_3 f^3 \tag{5.3}$$

  The short also has an associated delay for the same reasons as the open.

- Load – The Load is considered in the standard model as a perfect Load, so it have an $\Gamma_L = 0$ and zero delay.

- Thru – The Thru is considered as a perfect match, but with an electrical delay, characterized by its length[3].



(a) Coaxial Open Standard, from [6]

(b) Calibration Offset Equivalent Model

Figure 5.8

From the calibration parameters to the actual value on each measurement, further calculations may exist. The calculation of the C_k and $L_k (k = 0, 1, 2, 3)$ contribution to the final $\Gamma(f)$ is an easy task because the model parameters could be used directly. However, compute the delay contribution at each frequency requires more complex calculations. In the figure 5.8b could be observed the equivalent model of the open, that is valid to the short, too.

Final $\Gamma(f)$ values can be calculated for coaxial devices using the following equations derived from this model, from the transmission line equation $T = e^{(\alpha+j\beta)l}$ and from the definition of the specified offset loss (off_{loss}), offset delay(off_{delay}) and offset Z_0 (off_{Z0}).

$$\Gamma_{term} = e^{-2j\gamma_{off}}\,\Gamma_{model}\,, \quad \text{with} \quad \gamma_{off} = \alpha_{off} + j\beta_{off} \tag{5.4}$$

$$\alpha_{off} = \frac{off_{delay} \cdot off_{delay}}{2\,off_{Z0}}\sqrt{\frac{f}{10^9}}\,, \quad f \text{ in Hz}$$

$$\beta_{off} = 2\pi f \cdot off_{delay} + \alpha l$$

To perform measurements with the proposed instrument, two different PC3.5 type coaxial calibration kits were used, firstly the Agilent 85033D[52] and after the Agilent 85052D[53]. The information source to each calibration term parameter was the datasheet [52], in the first case and the Agilent website [54], in the last.

The TRL (Trough, Reflect, Line) is another very popular method to perform the calibration procedure on a VNA. It is based on different standards and used for non coaxial

[3]When test a DUT with the same type connectors and different genders, the 2 ports of the Analyzer could be directly connected. This produces a thru with 0 delay.

environments, such as wave-guides, non-incertable devices[4], or making on-wafer measurements.

Two types of error correction could be used to perform a VNA calibration, a response normalization correction or a vector error correction. The response correction is essentially a normalized calculation, where a reference measurement is performed and then the real DUT measurement is divided by the previous reference. This type of error correction is simple to apply, but only corrects some of the systematic measurement errors.

The most complete procedure is the vector error correction. It is based on linear vector error models in order to represent the real instrument imperfections. Using the standards presented before it is possible to know each of the model errors and further correction could be achieved. In figure 5.9 is represented the differences expected using the two error correction types, it is clear that the ripple effect presented on the normalized correction could be suppressed with the vector correction.

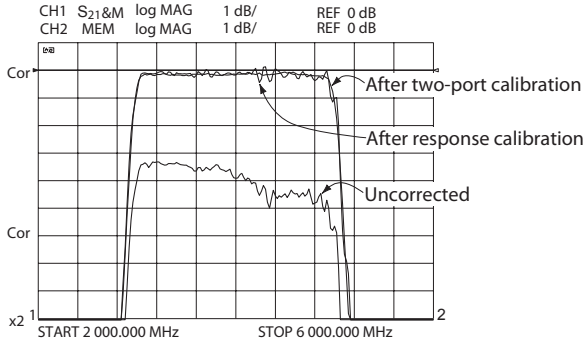


Figure 5.9: Normalizations response versus Vector Error Calibration results, from [7]

The two main techniques used to perform vector error correction were studied in order to use them on the proposed instrument and they will be described below.[5]

5.4.1 Analog One-Port Devices – 3-term technique

To perform accurate S_{11} measurements on one-port devices, such as an antenna, is enough to calibrate a VNA with the SOL (Short, Open, Load)[6] calibration process, as described on [55].

The equivalent signal-flow graph of the imperfections on one port, can be drawn as show on Figure 5.10a, from this, after some simplifications, the three unknown parameters can be extracted. These three error parameters are then used to correct the next measures with the DUTs.

From the figure 5.10a, to the figure 5.10b, the errors introduced on the forward incident branch, e_{10}, were incorporated in e_{01}. The notation used on Figure 5.10 are explained below:

- $\Gamma_M \rightarrow$ Measured S_{11}

[4]Devices with different connector types on each port, e.g. port 1: 2,94 mm connector, female; port 2: N-type connector, female.

[5]On [51] could be found much more informations about the way the calibration process is done in commercial VNAs.

[6]In some literature this technique can be referred as OSM (Open, Short, Match)

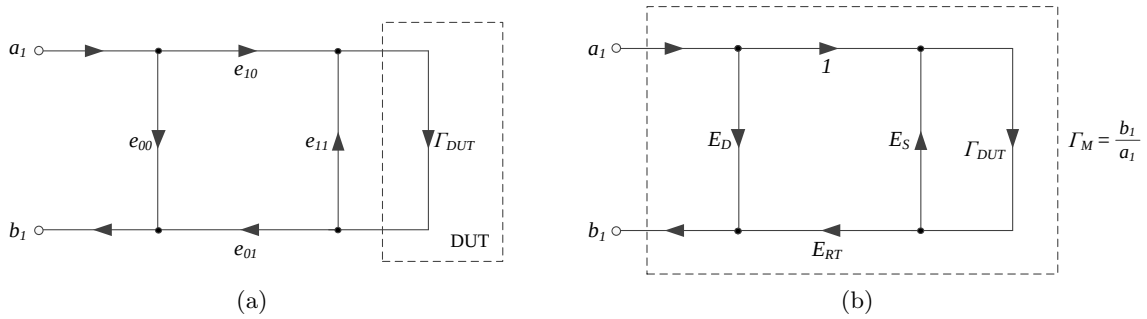


Figure 5.10: One-Port Calibration Imperfections

- $\Gamma_{DUT} \rightarrow$ Actual S_{11}
- $E_D = e_{00} \rightarrow$ Directivity Errors
- $E_S = e_{11} \rightarrow$ Source Match Errors
- $E_{RT} = e_{01}e_{10} \rightarrow$ Reflection Tracking Errors

Starting from the signal flow in figure 5.10b, several rearranges can be taken in order to arrive at the final expression in the equation 5.5. From this, a set of three equal equations can be expressed, each one to each calibration standard, where each Γ_{DUT} will correspond to the Γ of the corresponding calibration standard. To realize the previous process the right reflection coefficient value for each calibration standard must be known. This can be accomplished using the models presented before for the wanted measurement frequencies.

$$\Gamma_M = E_D + E_{RT}\left(\frac{\Gamma_{DUT}}{1 - E_S\Gamma_{DUT}}\right) \tag{5.5}$$

The solution of the system can provide the result to the three unknown errors. To simplify the computation of the results, an algorithm to sequential solve the system of equations was written and implemented on MATLAB®.

The correction of further measurements is done using the three error values calculated, on the equation 5.5 but in order to the Γ_{DUT}.

5.4.2 Analog Two-Port Devices – 12-term technique

This technique is used on traditional VNAs that only have one generator, so to completely characterize a two port component, they need an additional switch to alternate between the ports. To fully-correct the two-ports of the VNA the 12-term techniques uses two similar error models, one to each way of the measurement. The error signal flow to one port could be represented as on figure 5.11.

As for one-port devices, after a simplification of the model, each parameter could be calculated from a set of equation. Those equations could be found on [56]. Then, with the right set of standard calibration measurements vectorial results are found. Thus they could be used in the same way they were calculated to calibrate further measurements.

In the proposed instrument are presented the same non-idealties as on the model of the 12-term technique. Besides, a simplification could be made, because the cross-talking parameter

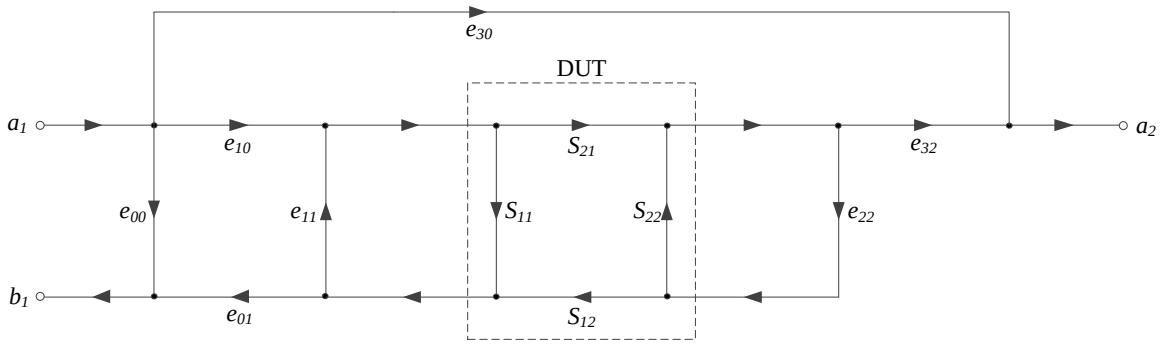


Figure 5.11: 12 term imperfection signal flow

that characterizes the switch non-idealities is not applied there and could be left out. So the intention is to use this model in order to obtain a valid and complete calibration method.

However, in the proposed instrument the S_{21} measurement is relative, the absolute phase is not known due to the implemented 2-tone technique, as explained before on chapter 5.2.1. This makes the intention of use 12-term calibration procedure to fail. It is used on traditional VNA measurements, where the an absolute measurement is always preformed and so it uses complex calibration values to correct the measured ones. In other words, the 12-term calibration procedure needs absolute measurements to be performed.

In conclusion the alternative is to use a simple response normalization to correct the gain of two-port analog devices and the previous 3-term technique to correct the S_{11} measurements. This correction leads to poorer results, but without at least a third superhetherodyne receiver an one-tone characterization could not be performed and so, this is the only option to perform a calibration on these devices.

5.4.3 Mixed-Domain Devices

To perform the calibration on Mixed-Domain Devices will be done the same approach used for 2-port Analog Devices. Which means, the use of the 3-term technique to correct S_{11} measurements and the use of normalization response to correct S_{21} measurements.

Nevertheless, the typical example of mixed-domain devices are ADCs or DACs, which contrary to 2-port analog devices, are unilateral devices so, no energy will flow back from the second to the first port, i.e. they have an $S_{12} = 0$. Furthermore in the ADC case its second port is digital so, it is assumed that it as an ideal adaptation, which means an $S_{22} = 0$. Thus with this two characteristics, intuitively is easy to denote that, at the analog port looks like an one-port device, the amount of energy reflected is only due to the S_{11} of the device. So, the 3-term technique should be enough to perform fully accurate S_{11} measurements. To prove it, the S_{11} equation error derived from the 12-term error model, presented on 5.6, was used. Then using 0 for all the S_{12} and S_{22} values, the equation 5.7 will be found, which is equal to the equation 5.5.

$$S_{11M} = e_{00} + (e_{10}e_{01})\frac{S_{11} - e_{22}\Delta_S}{1 - e_{11}S_{11} - e_{22}S_{22} + e_{11}e_{22}\Delta_S}\ , \quad \text{with} \quad \Delta_S = S_{11}S_{22} - S_{21}S_{12} \tag{5.6}$$

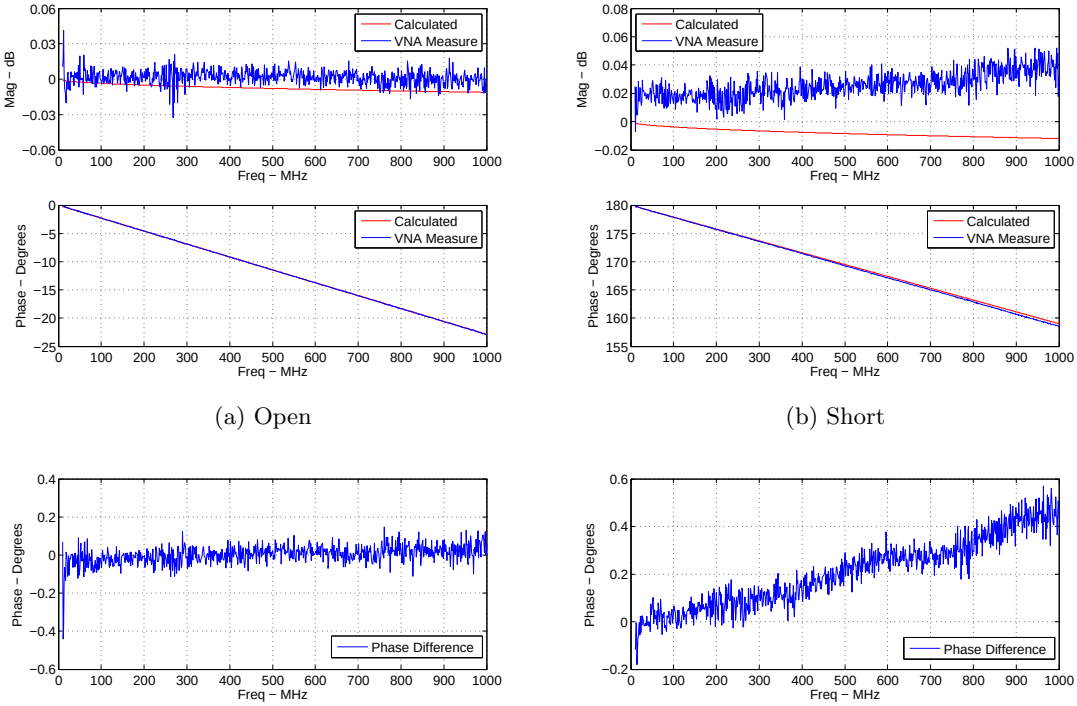
$$\text{If, } S_{12} = 0 \text{ and } S_{22} = 0 \quad \Rightarrow \Delta_S = 0 \quad \Rightarrow S_{11M} = e_{00} + \frac{(e_{10}e_{01})S_{11}}{1 - e_{11}S_{11}} \tag{5.7}$$

This means that using the 3-terms technique to calibrate mixed-domain devices is enough to correct for the systematic errors, which affect the S_{11} readings.

The S_{21} measurement is a different case. To fully correct this measurement, a vector error correction will be needed. As, the use of the normalization response will not provide for the correction of all the systematic errors present in this measurement, some ripple is still possible to appear on the magnitude gain results, but nothing could be done in this matter for now.

5.4.4 SOLT Terms Parameters Confirmation

To evaluate the parameters used to model SOLT standards. Each one had been measured in the VNA. After a correct calibration procedure, the measurement result for each standard should be exactly the standard model itself.



(a) Open

(b) Short

(c) Open Difference from VNA

(d) Short Difference from VNA

Figure 5.12: Open and Short Standards response comparison

The results for the Open and Short Standard are shown in figure 5.12. The Magnitude results from the VNA are almost only noise, because the both terms are very close to the ideal. So, the calculated parameters are for sure right. The Phase results are the most important ones, and here at a first glance the calculated values seem to match the values used by the VNA. In the figures 5.12c and 5.12d the difference between the calculated phase and the VNA measured phase are depicted. Good results are shown with a deviance lower than 0,6°, for the Short.

The results for the Load Standard are not depicted, but the results from the VNA matched the calculated response, apart from the expected noise. So the ideal proprieties assumed to the Load are confirmed.

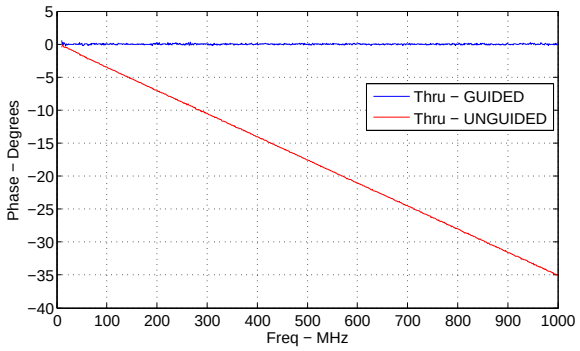


Figure 5.13: Thru Standard Measured on Agilent PNA E8361C

The Thru Standard are described in the Measurement Kit Specifications as an ideal Thru, therefore without attenuation or delay. However in the VNA used to compare the results, the Agilent PNA E8361C, has two calibration option, the "GUIDED" option and the "UNGUIDED", both allows the user to perform a complete 2-port calibration using SOLT Standards. But, the strange fact is that the "GUIDED" calibration option in the end of the calibration suggest a delay for the thru measurement. The results in the VNA referred, with the same calibration kit, with the same thru standard are depicted on figure 5.13.

Indeed the delay suggested in the end of the calibration procedure is the value used by the VNA to perform the corrections. The value for the measurements done is around 0,094 ns. Although, the way how the VNA calculates the delay remains unknow, the fact is that the measurements performed on the VNA with the "GUIDED" option and accepting the delay suggested result in better results with much less ripple.

To perform the measurements with our instrument the delay used for the thru Standard was 0. It was considered as an ideal thru as in its specifications. Until now for our instrument the calibration process is an one way process, it only allows to correct for the system imperfections if the specific characteristics of the calibration terms had been known. It can't be applied on the revers direction. However the results on the VNA considering the non-zero delay are for sure closer to the real response of each component tested. So the VNA results taken for comparison had been performed using the "GUIDED" calibration option and a delay mismatches close to the value on the figure 5.13, -35° are expected

5.5 Graphical User Interface

In order to provide an easy to use instrument interface, a simplistic Graphical User Interface (GUI) was created in the MATLAB®environment. In the GUI the user has available the definition of the measurement parameters, the calibration steps and the visualization of the results in the common formats.

The initial menu could be depicted in figure 5.14. In it, the user may choose the type of measurement to perform and the format it will be displayed.

A menu to set the measurement parameters was also produced, it is shown on figure 5.15a. This is a very important menu, it is able to change some of the parameters in order to avoid stimulus signals that could produce frequency response anomalies. When the user presses the "`Correct`" button, one of the parameters will be altered, if necessary. With this option, the

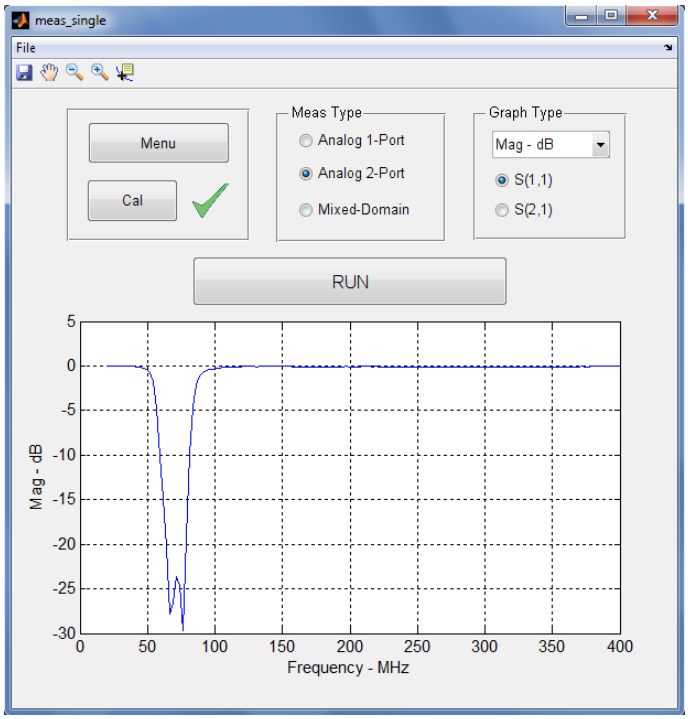


Figure 5.14: GUI Main menu – entry menu

system will prevent two anomalous cases.

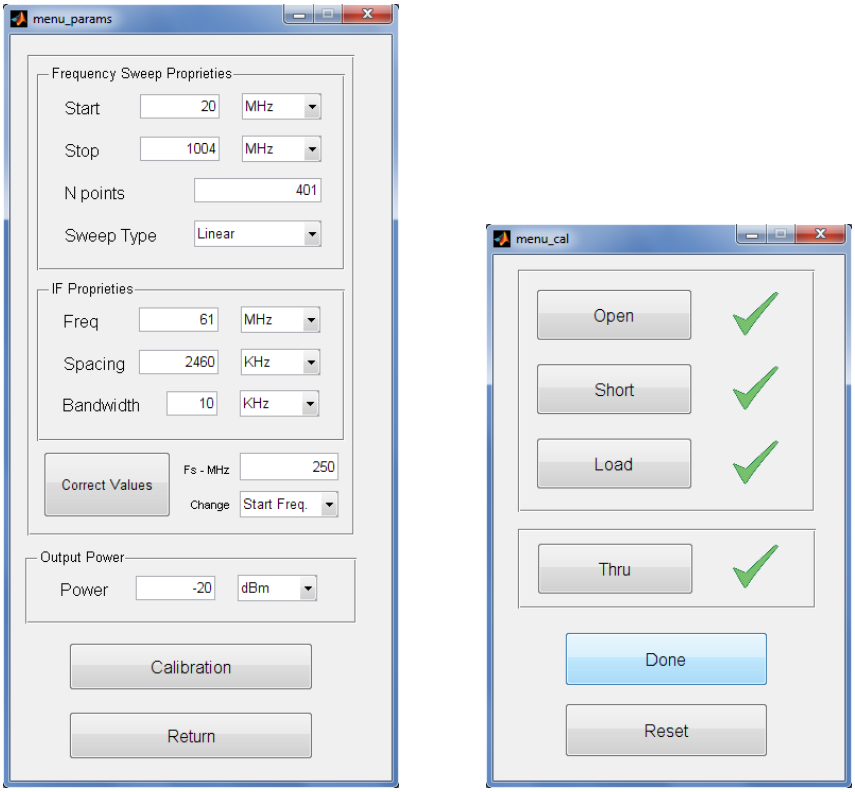
In the first place stimulus frequencies that coincide with a multiple of $\frac{1}{3}f_S$ or $\frac{1}{4}f_S$ are avoided. As these frequencies are multiples of the sampling frequency, in each period of the input signal the samples will be taken always in the same location, in the cases referred will only be taken 1, 2, 3 or 4 samples per period, which result in a mismatch when the power of the stimulus frequency has to be computed. For higher frequency sampling multiples mismatches will also occur, but will have much less impact on the measure. Because of that only these multiples were cared of.

In the second place, when performing measures with two tones, cases where the tones stay at the same distance from the same Nyquist band separation will be avoided. Because if this happens, in one measure step, over-position of the two tones will exist and the information of each one will be destroyed.

This anomalous cases only happens on the ADC under test, because it is been fed directly. The incident and reflected signals are been received through the super-heterodyne paths so, those issues will not occur.

To automates the calibration process another menu was produced. It was represented on figure 5.15b. As found on traditional VNAs this menu provide for a reading of each one of the SOLT standard terms. An alteration in the measurement parameters of the previous menu means that the calibration is no longer valid and so this menu alerts the user for that occurrence.

A detailed User's Manual could be found on chapter B.



(a) GUI – Parameter menu (b) GUI – Calibration menu

Figure 5.15: GUI Sub menus

Chapter 6

Results

Several measurements to evaluate the performance of the instrument are presented. Whenever it was possible the results were compared with the results from the commercial VNA Agilent PNA E8361C. Both instruments were calibrated with the same calibration kit, the Agilent 85052D[53] and operated within the same measurement conditions, such as number of points and frequency sweep parameters. All the DUTs measured have SMA connections.

6.1 Analog Devices

All the S_{21} and S_{11} achieved results were compared with the results obtained on the Agilent VNA.

All the devices are 2-port devices and all the results presented were taken using a 2-tone signal as the stimulus signal, even to measure the S_{11}. All the measurements were performed in the full frequency capability of the instrument, from 20 to 1004 MHz with 401 points and thus a frequency space of 2,46 MHz. The input power of the first tone was equal to the input power used to measure the results on the Agilent VNA. The input values used were -10 dBm in the majority of the measurements and -20 dBm in the case of the Amplifier Avago ABA53563.

6.1.1 Low pass filter

S11

The first S_{11} traces shown here, follows quite good the one from the VNA.

The magnitude Error was below 0,7 dB in all the frequencies.

In the phase Error an growing value can be denoted, that culminates with 40° error. This error is not expected, since the standard term verification for the open, the short and the load are fine. Although it's source remains unknown, the error exist.

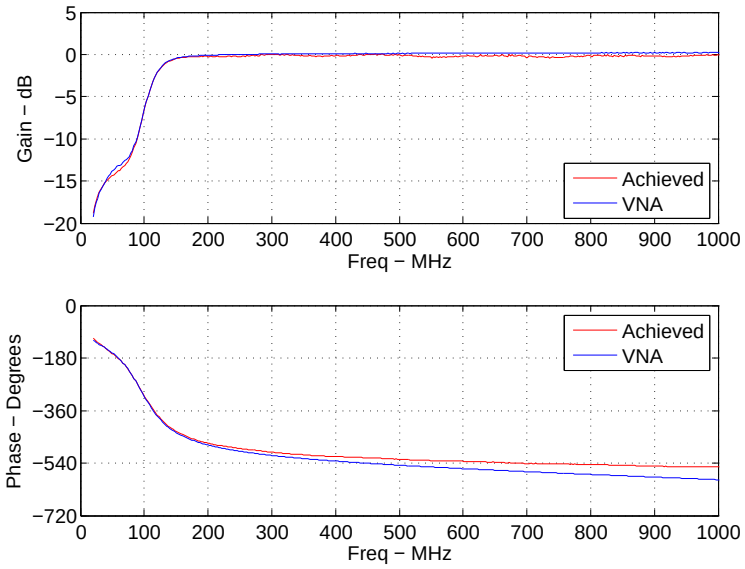


Figure 6.1: S_{11} of a common LPF – 20 to 1000 MHz

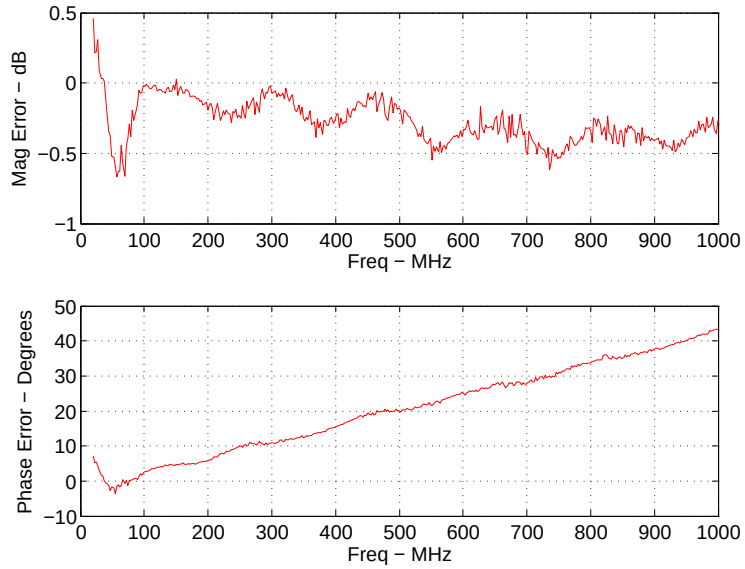


Figure 6.2: S_{11} Error of a common LPF – 20 to 1000 MHz

S21

The general gain trace closely follows the VNA results. Only for high attenuations values a mismatch can be denoted, due to the limited dynamic range of the instrument compared to the VNA.

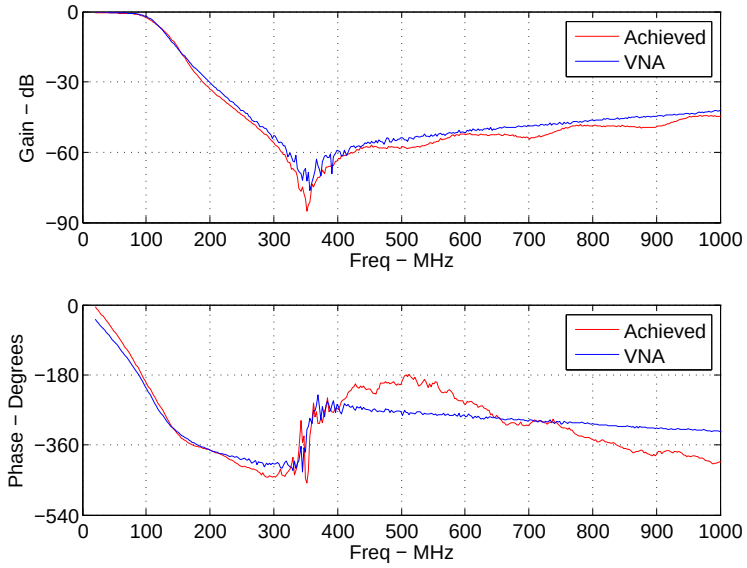


Figure 6.3: S_{21} of a common LPF – 20 to 1000 MHz

At frequencies where the filter still has low attenuation (lower than 20 dB, the results shows good accuracy, with 1 dB magnitude error.

The phase results had a growing behaviour that ends with $-60°$ error, which was already expected, due to the 0 delay considered for the thru (section 5.4.4.

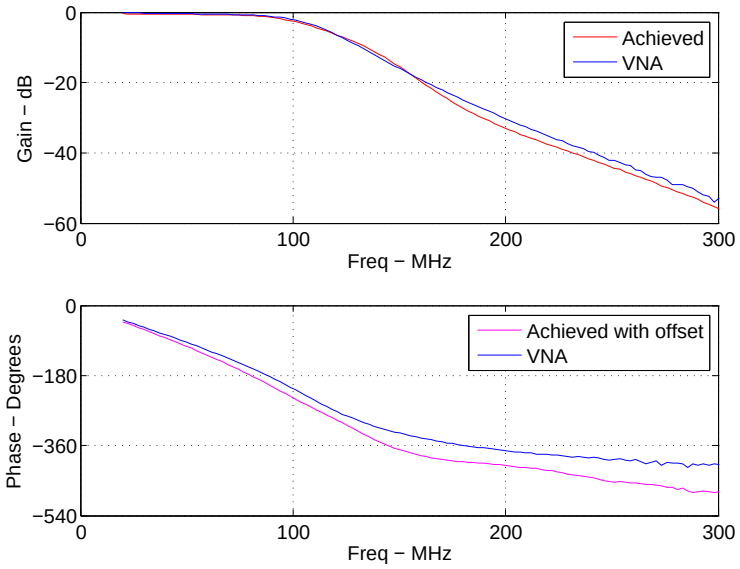


Figure 6.4: S_{21} of a common LPF (detail) – 20 to 300 MHz

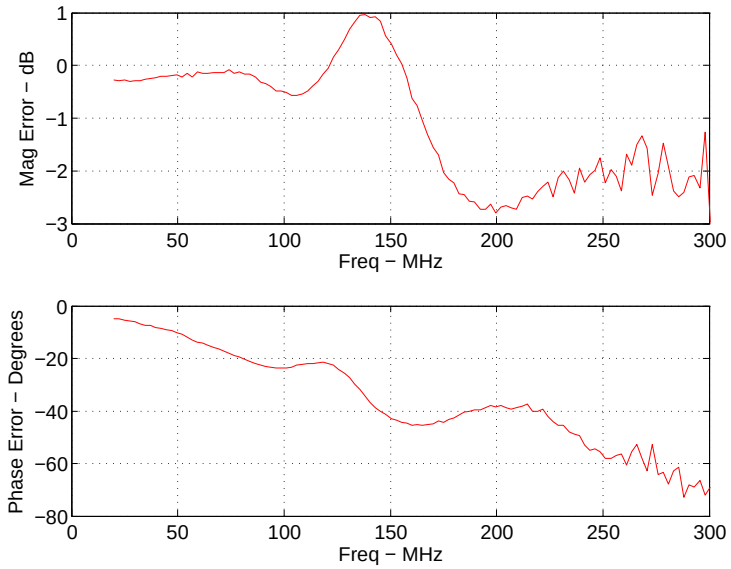


Figure 6.5: S_{21} Error of a common LPF (detail) – 20 to 300 MHz

6.1.2 Band Pass Filter 1 – MiniCircuits SBP-70+

The Mini-Circuits [57] BPF was tested also.

S11

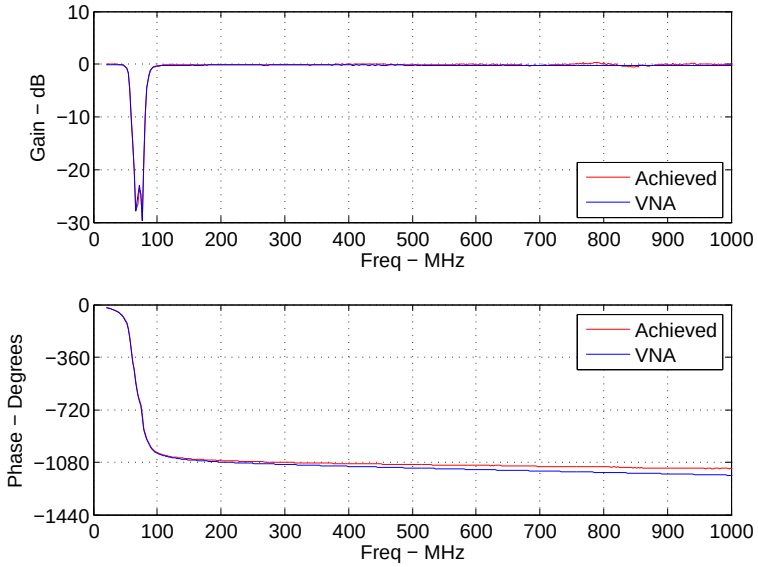


Figure 6.6: S_{11} of the BPF SBP-70+ – 20 to 1000 MHz

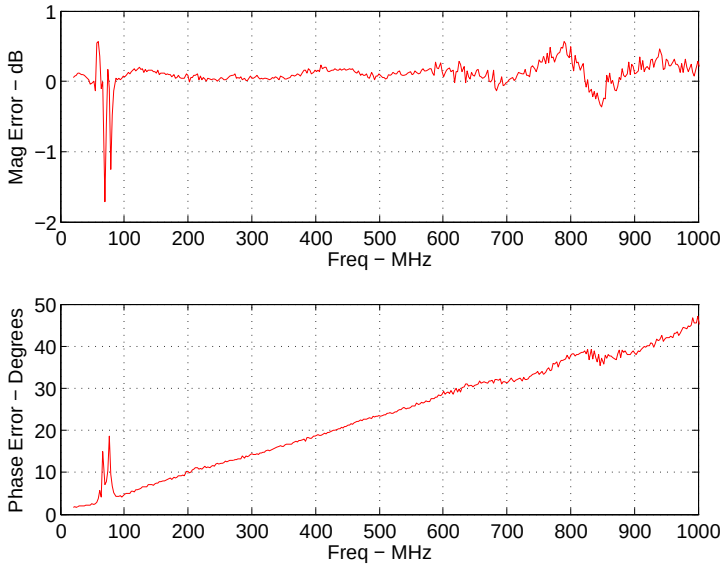


Figure 6.7: S_{11} Error of the BPF SBP-70+ – 20 to 1000 MHz

Once again the S_{11} magnitude results shows very good accuracy against the VNA results.

Only with errors of 1 dB on the filter's pass band, where the return loss value is too low.

The phase results shows again the same growing phase error seen in the first component and the end value is also around 40 dB.

S21

The accuracy was quite good, with some errors appearing only on the stop band of the filter, due to the high attenuation.

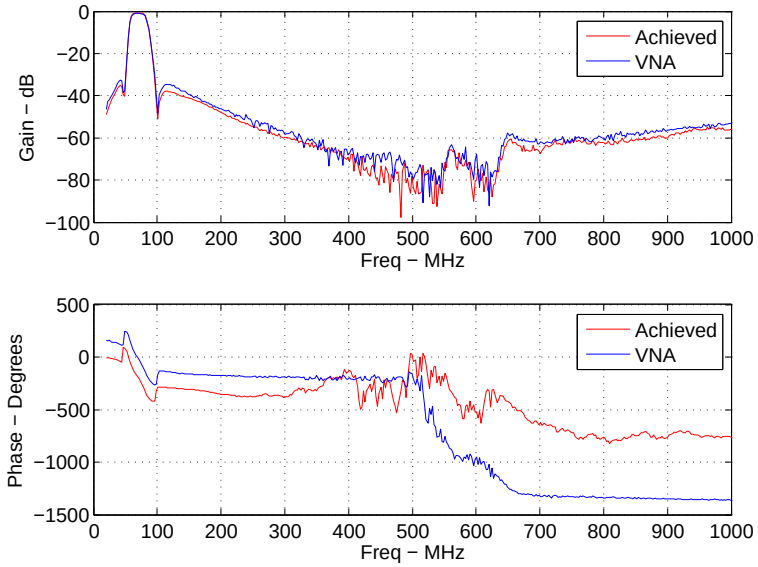


Figure 6.8: S_{21} of the BPF SBP-70+ – 20 to 1000 MHz

With the phase of the VNA first point, an offset was added to the two tone result measured, because it was assumed to be 0°. The phase trace shown in detail in figure 6.9 was faithfully reproduces the phase of the filter around the pass band.

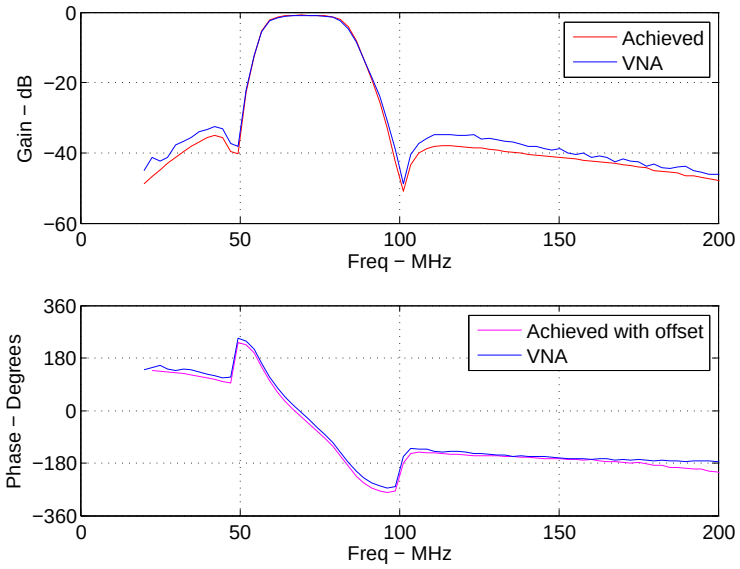


Figure 6.9: S_{21} of the BPF SBP-70+ (detail) – 20 to 200 MHz

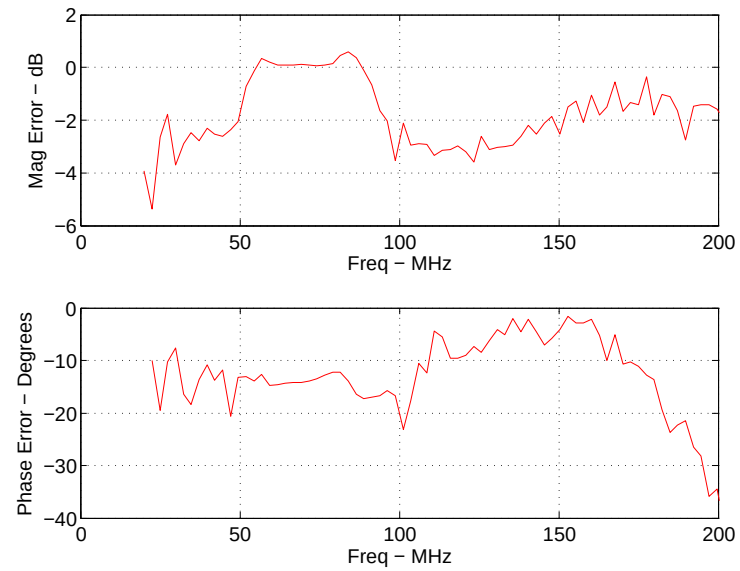


Figure 6.10: S_{21} Error of the BPF SBP-70+ (detail) – 20 to 200 MHz

6.1.3 Band Pass Filter 2 – IF Filter (Details on section 4.2.4)

S11

More very good S_{11} results, with the same phase error seen before.

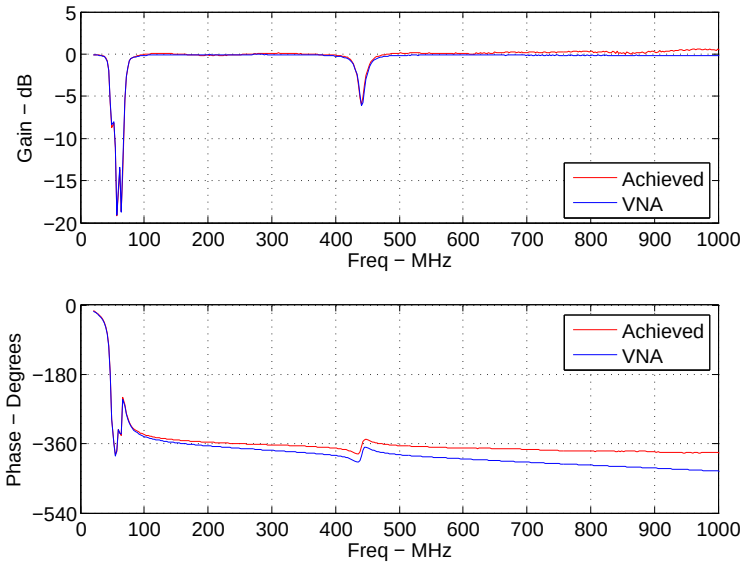


Figure 6.11: S_{11} of the IF BPF – 20 to 1000 MHz

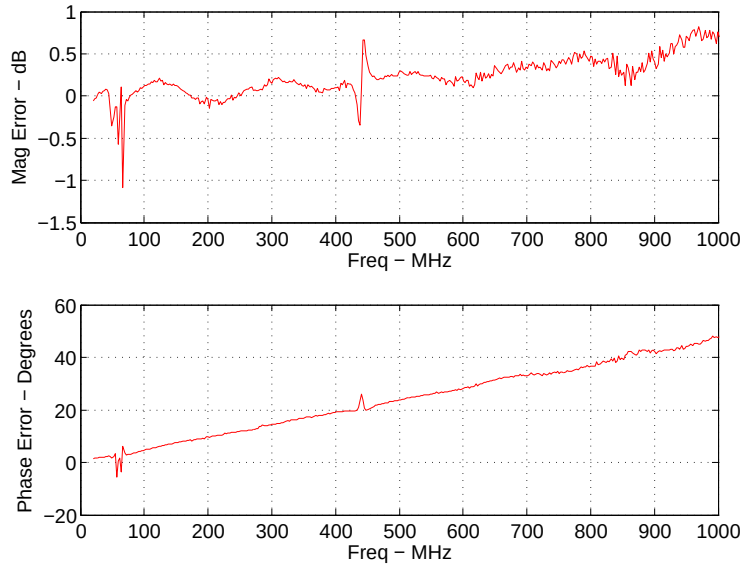


Figure 6.12: S_{11} Error of the IF BPF – 20 to 1000 MHz

S21

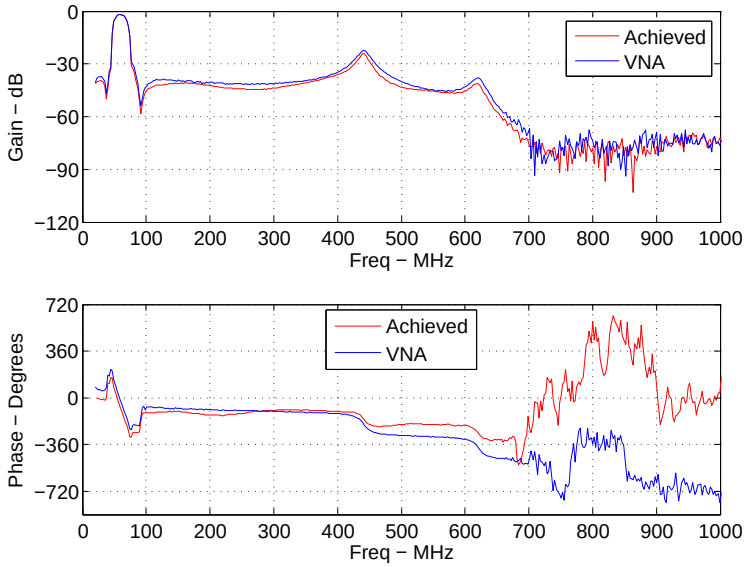


Figure 6.13: S_{21} of the IF BPF – 20 to 1000 MHz

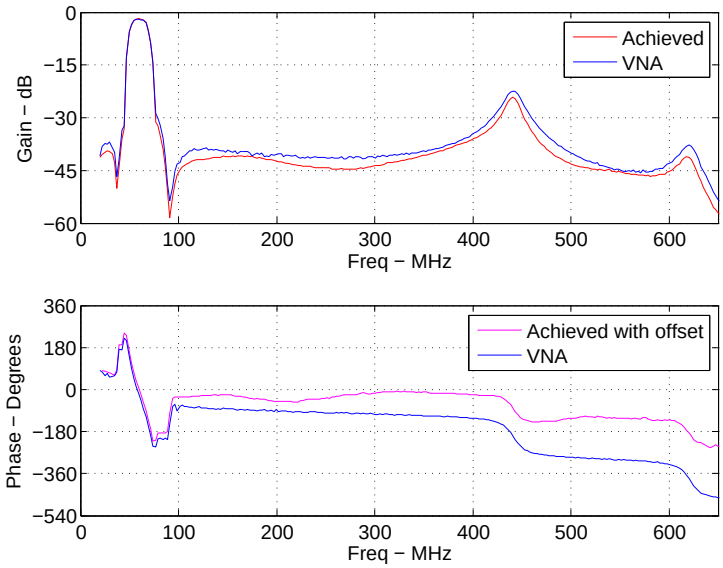


Figure 6.14: S_{21} of the IF BPF (detail) – 20 to 650 MHz

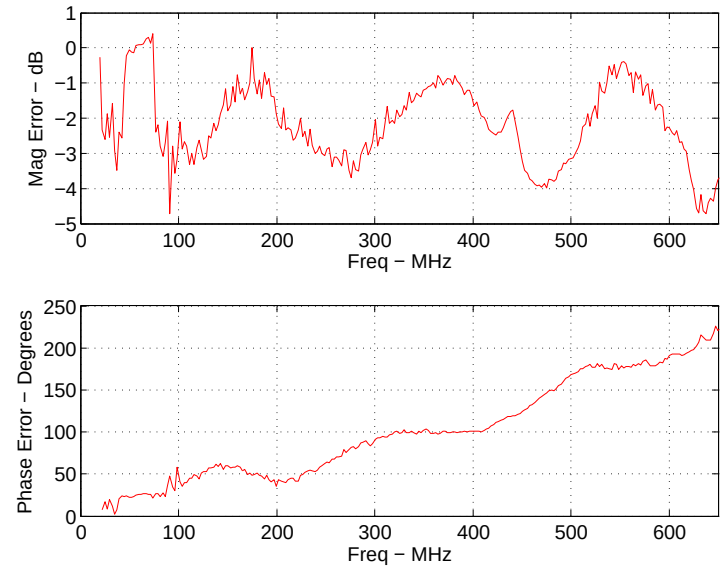


Figure 6.15: S_{21} Error of the IF BPF (detail) – 20 to 650 MHz

6.1.4 Amplifier – Avago ABA53563

The amplifier Avago ABA53563[28] used on section 4.2.5 was tested here with the board built there.

S11

The S_{11} of the amplifier was the worst until now, nevertheless the magnitude error never goes up the 2,5 dB. This result is once more due to the low dynamic range of the instrument, since the return loss of the amplifier is much lower then the values measured in the last components.

The phase mismatch seen in the last S_{11} results is once again present in the measure.

S21

The S_{21} results denotes some ripple, as expected, in spite of the calibration procedure used. However the magnitude error values are quite good with less than 0,5 dB of error in all the band.

The missalignment of the phase is also expected.

S21 – Validate thru influence

In order to validate the assumed bad influence of the thru standard on the S_{21} results, a calibration was performed using an ideal thru, i.e. using two cables with different gender. Then, this calibration was applied to a measure of the ABA53563 with an male to male SMA adapter on the output port. The VNA results for comparison was also performed to the same set (ABA53563 + output adapter).

S11

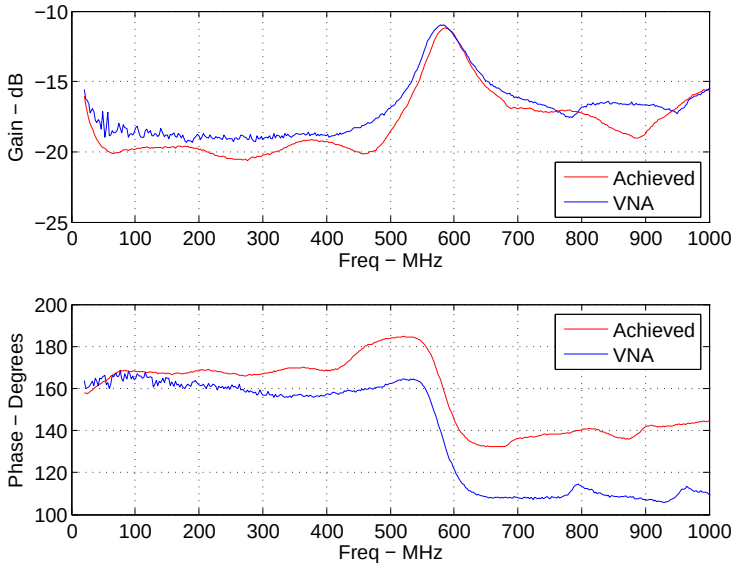


Figure 6.16: S_{11} of the ABA53563 – 20 to 1000 MHz

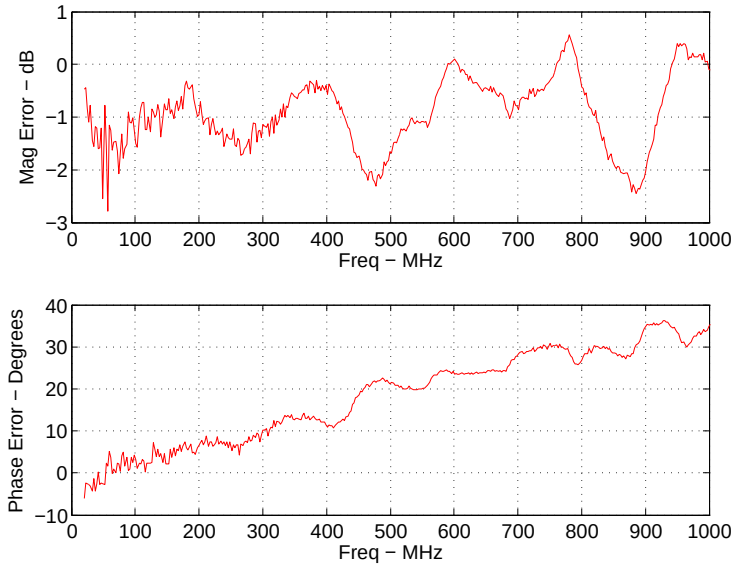


Figure 6.17: S_{11} Error of the ABA53563 – 20 to 1000 MHz

S21

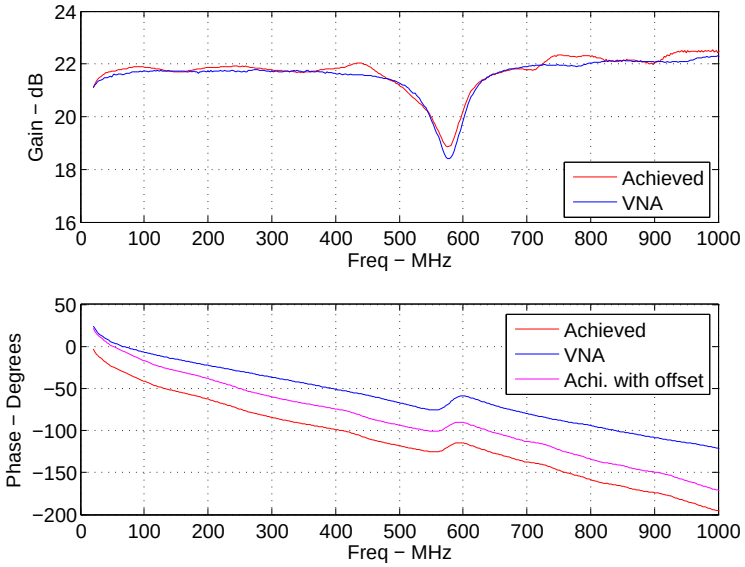


Figure 6.18: S_{21} of the ABA53563 – 20 to 1000 MHz

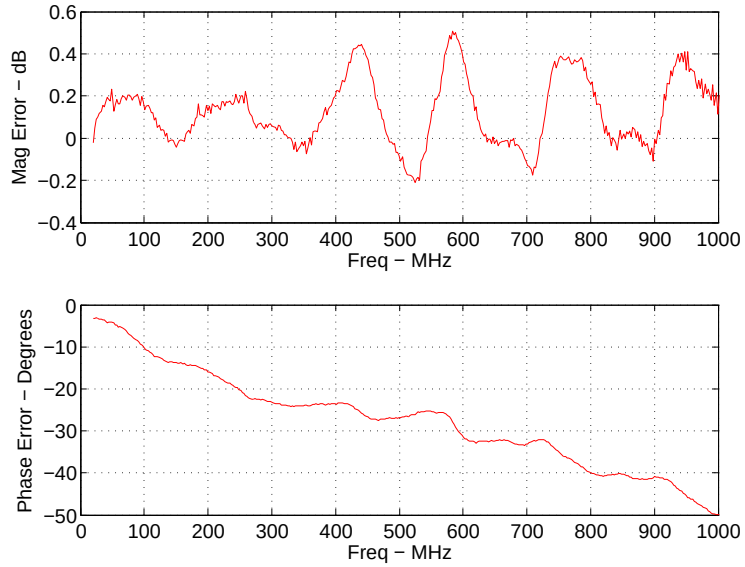


Figure 6.19: S_{21} Error of the ABA53563 – 20 to 1000 MHz

S21 – Validate thru influence

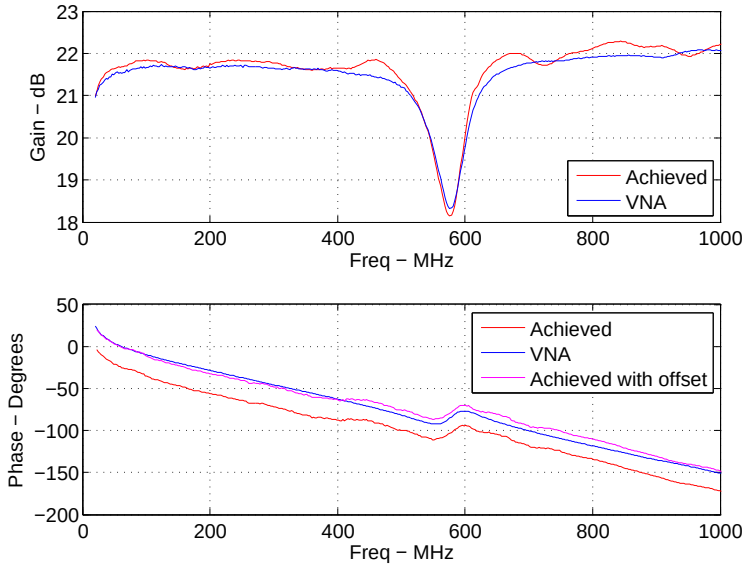


Figure 6.20: S_{21} of the ABA53563 plus output adapter – 20 to 1000 MHz

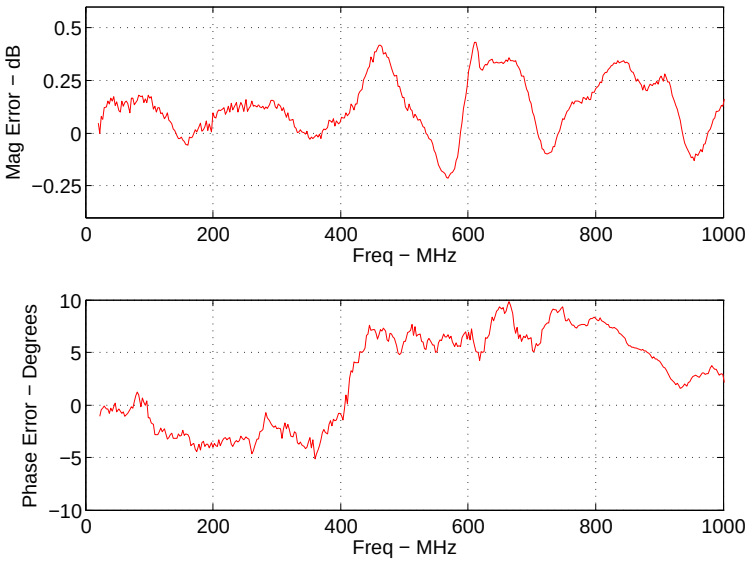


Figure 6.21: S_{21} Error of the ABA53563 plus output adapter – 20 to 1000 MHz

6.2 Mixed-Domain Devices

6.2.1 ADC – TI ADS5521EVM

S11

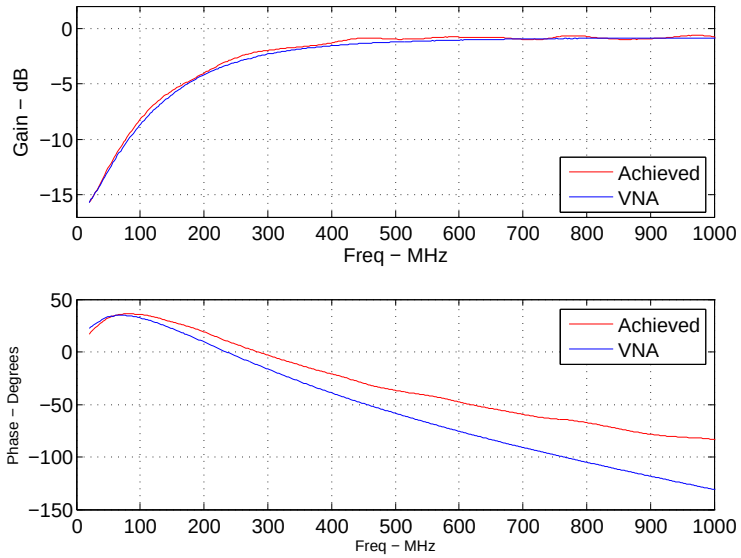


Figure 6.22: S_{11} of the ADS5521EVM – 20 to 420 MHz

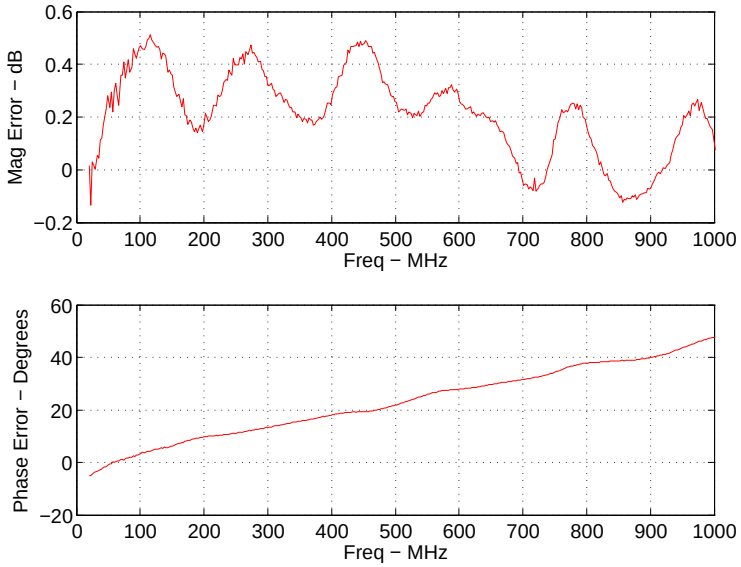


Figure 6.23: S_{11} Error of the ADS5521EVM – 20 to 420 MHz

The S_{11} of the ADS5521EVM[58] was taken with the one-tone measure, from 20 to

1004 MHz and with -10 dBm input power. Both results, from the instrument and from the VNA, were measured with the ADC working at a f_S of 101.3 MSPS.

As expected the S_{11} results had a very good correspondence with results from the VNA. The same phase error seen on the previous results was denoted.

S21

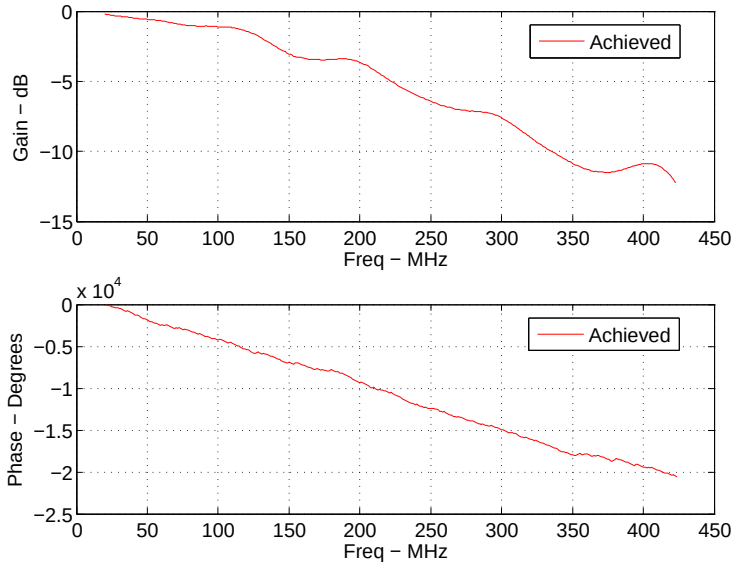


Figure 6.24: S_{21} of the ADS5521EVM – 20 to 420 MHz

To validate the truth of the ADC Gain measurements, the Mini-Circuits filter SBP-70+, already measured before, was placed before the ADC input. Between the two was also placed an 1 dB attenuator.

S21

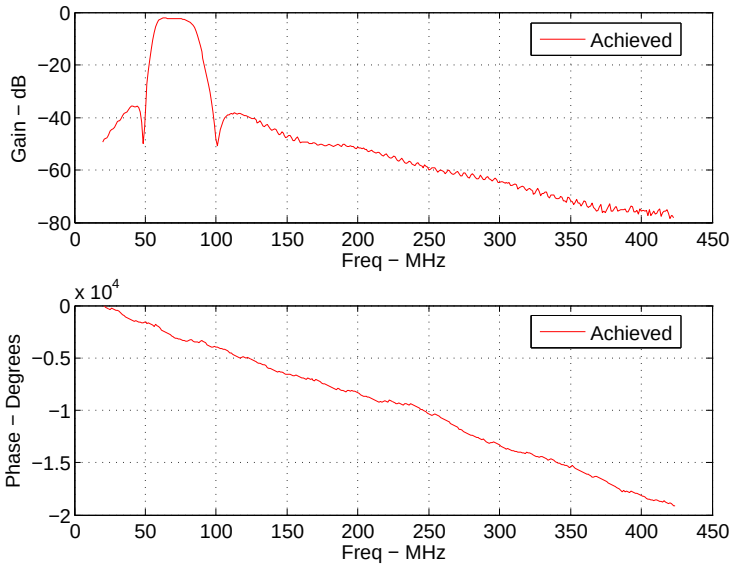


Figure 6.25: S_{21} of the set SBP-70+ - 1 dB atten. - ADS5521EVM – 20 to 420 MHz

The magnitude results are according to the expected. Due to the low attenuation of the ADC on the measured band, comparatively with the attenuation of the filter, the amplitude response obtained now, was very close to the response of the filter itself.

The ADC phase delay value is several orders higher than the phase delay of the filter, this way, its effects could be hidden in the graph. To discover it, the measurement done for the ADC alone was treated as the reading of calibration thru result and the result with filter as the measurement to correct. Then, a normalization procedure is applied to both measurements and the filter phase response should appear as the result. But this is not what happens. The phase results are not the expected ones, because the phase doesn't reflect the addition of the filter on the chain.

The phase obtained is not shown, but it is much like the result on figure 6.24. This means that the ADC phase delay readings are not correct.

To evaluate this problem the ADC was fed by the same frequency two-tone signal 100 times. The phase delay between the two tones from the ADC was then compared with the phase from the oscilloscope. The generator will send the trigger signal, in almost the same instant, so the result should be an almost constant phase delay at every measurement points. Even if it is not like this, a relation between results must exist. As could be seen on figure 6.26, while the oscilloscope give almost the same phase value, the ADC measurements seem to change 180° very often. It could be easily understood, that this is the source of the error.

The origin of the error could be in two places, in the ADC input circuitry, which is not likely. If this was the source of the error, it has to have a random behaviour, due to the non-relation with the oscilloscope observed. Then, the measurement was repeated for two ADS5521EVM ADCs, receiving the approximate same signal through a resistive splitter. The results revealed, as it has to be, the same results between ADCs and the same anomalous behaviour between each ADC and the oscilloscope.

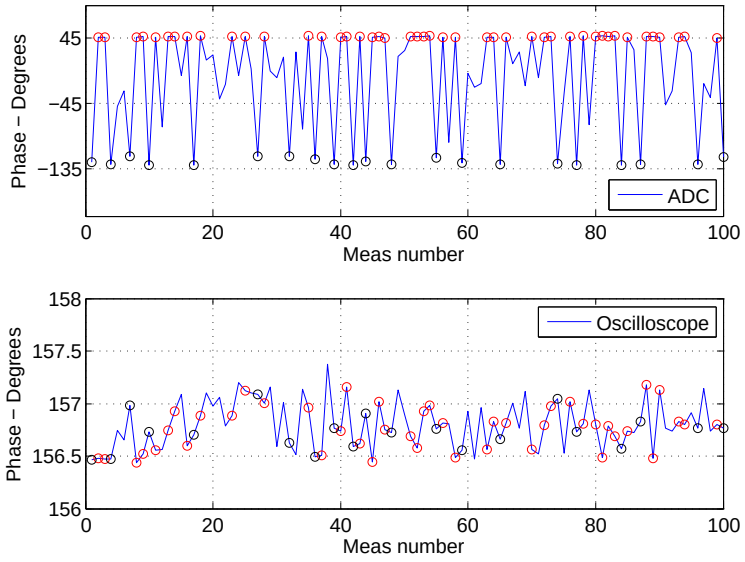


Figure 6.26: Result from the ADC phase test, f_{in} =40 and 40,5 MHz, $f_{S\ \mathrm{ADC}}$ =101.3 MSPS, $f_{S\ \mathrm{OSC}}$ =250 MSPS

This way, the most probably origin of the error is in the synchronism between triggers. If the LA trigger is not synchronous with the oscilloscope trigger, phase mismatches will occur. In this case phase errors will have a random behaviour, as seen here.

Even if the reader, at this time, believes that the source of the error was in the two different sample rates of the ADC and the oscilloscope, this assumption is not right, due to the characteristics of the two-tones technique, already mentioned on section 5.2.1. The performed phase measurements relates the phase of each tone and in this measure, the tones are spaced by 500 kHz (Δf), this value means that the phase relation between the two tones will rotate 360° every $T_{\Delta f} = 2\,\mu$s. The two sampling frequencies are $f_{SADC} = 101,3$ MSPS and $f_{SOsc} = 101,3$ MSPS. In the worst case scenario, the maximum time error in the first sample between the ADC and the Oscilloscope will be the sampling period of the lower sampling frequency.

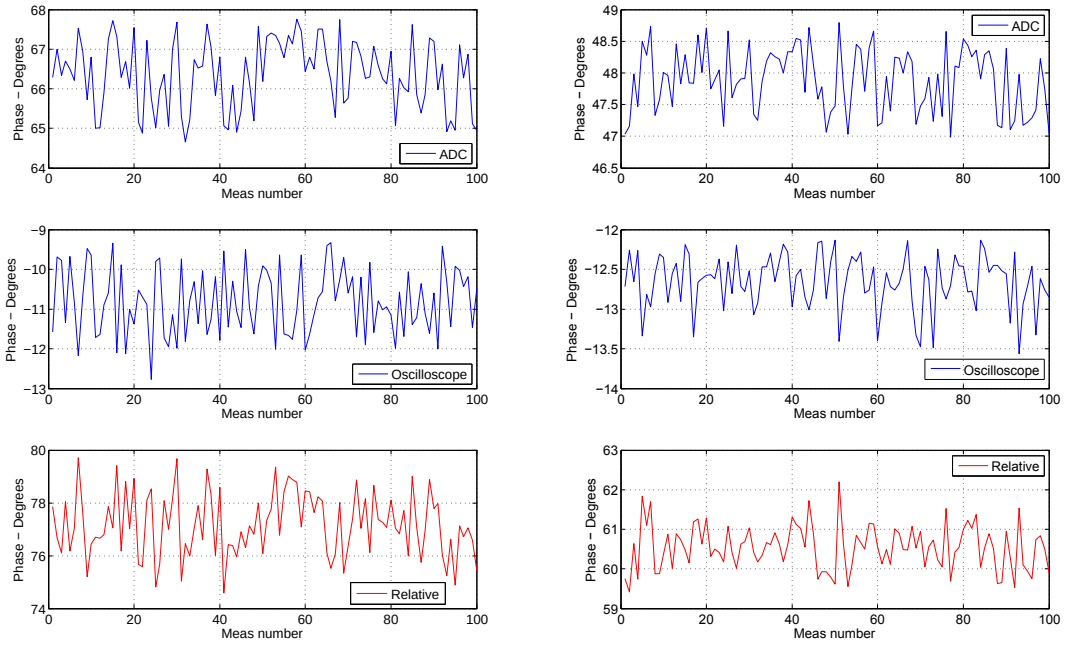
$$T_{S\ \mathrm{ADC}} = \frac{1}{101,3\,\mathrm{MSPS}} = 9,9\,\mathrm{ns} \qquad T_{S\ \mathrm{Osc}} = \frac{1}{250\,\mathrm{MSPS}} = 4\,\mathrm{ns}$$

$$\text{Phase Uncertainty} = \frac{min(T_{S\ \mathrm{ADC}}, T_{S\ \mathrm{Osc}})}{\frac{T_{\Delta f}}{360}} = 1,78° \tag{6.1}$$

In this case the phase uncertainty due to the non-synchronization of the sampling clocks will be 1, 78°.

Reconfigure Logic Analyzer Trigger

To avoid the use of the External Logic Analyzer trigger, an empty pin on the pod connected to the ADC was fed with the trigger signal. The results with this trigger were much closer to the expected. The repetition of the last test reveals now, a concordance between the relative phase of the tones on the oscilloscope and on the ADC. The results are shown on figure 6.27.



(a) $f_{S\ \mathrm{ADC}} = f_{S\ \mathrm{OSC}} = 65\,\mathrm{MSPS}$ (b) $f_{S\ \mathrm{ADC}} = 101.3\,\mathrm{MSPS}$, $f_{S\ \mathrm{OSC}} = 250\,\mathrm{MSPS}$

Figure 6.27: ADC Phase test with LA trigger in Bit, $f_{in} = 40$ and $40{,}5\,\mathrm{MHz}$

To validate the previous explanations about the phase uncertainties in this phase measurements, two tests were done. One with the ADC and the Oscilloscope at the same sample rate, $62{,}5\,\mathrm{MHz}$, shown on figure 6.27a. Another with the ADC at a sample rate of $101{,}3\,\mathrm{MHz}$ and the Oscilloscope at $250\,\mathrm{MHz}$ (the same configurations as before), shown on figure 6.27b. Both tests were performed with a two tone signal spaced by $500\,\mathrm{kHz}$. As could be denoted and as explained, the second case presents a little less variation than the first, due to the lower phase uncertainty. With the equation 6.1, could be calculated an uncertainty of $2,88°$ for the first case and $1,78°$ for the second one, which match the results presented.

The magnitude and phase result of the ADC S_{21} from 20 to $210\,\mathrm{MHz}$ is presented in figure 6.28, once again to confirm this results, an arrange with the SBP-70+, the ERA-4+ and a $6\,\mathrm{dB}$ attenuator, was placed right before the ADC input and the measure was calibrated in response. The results from this arrangement are shown on figure 6.29, this time the phase results show, without question, the VNA measure of the arrangement alone, which confirms the phase results from the ADC.

With the phase confirmation, a deeply analysis to the result could be done, as can be seen the ADC has a linear decreasing phase. The group delay imposed by the ADC can be

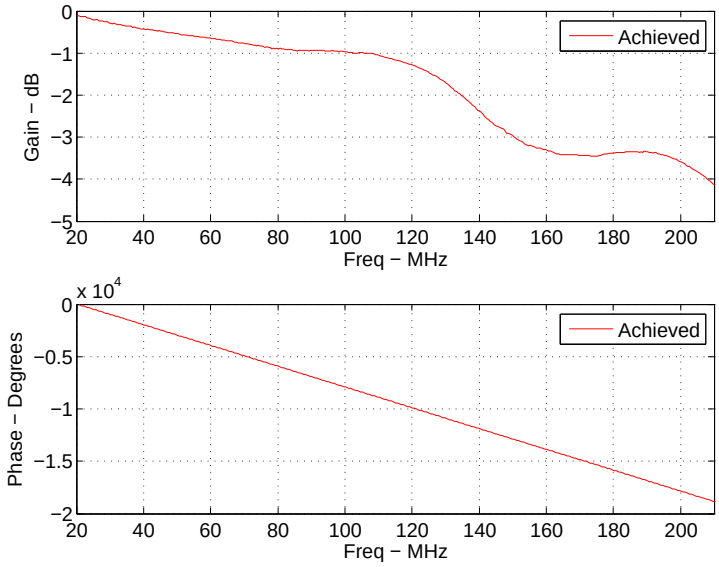


Figure 6.28: S_{21} of ADS5521EVM with LA trigger in Bit – 20 to 210 MHz

computed with the derivative of the phase, which in this case is simple to obtain. The first point of the trace was assumed to be 0° and the last point is nearly 18870°, the calculation can be done in the following way:

$$\tau_{gr} = \frac{1}{360}\frac{18870}{(210e6 - 20e6)} \approx 276\,\text{ns}$$

With the datasheet of the ADC IC, the TI ADS5521[59], was possible to know that a sample takes 17,5 clock cycles to propagates from the input to the output. Considering the sampling frequency of the test, the propagation time of the ADC was $17,5 \times \frac{1}{62,5e6} = 280\,\text{ns}$. Although the previous results aren't exactly in accordance with this value, the approximation between them is very high.

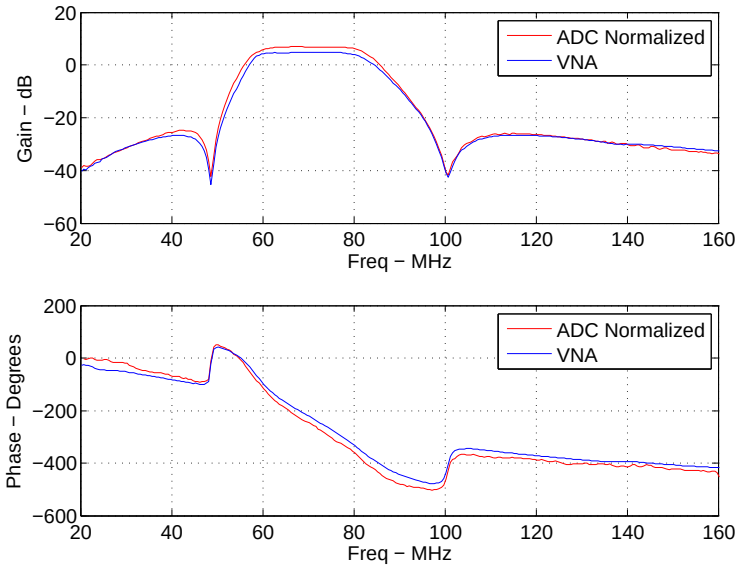


Figure 6.29: S_{21} of the set SBP-70+ - 1 dB atten. - ADS5521EVM with LA trigger in Bit – 20 to 160 MHz

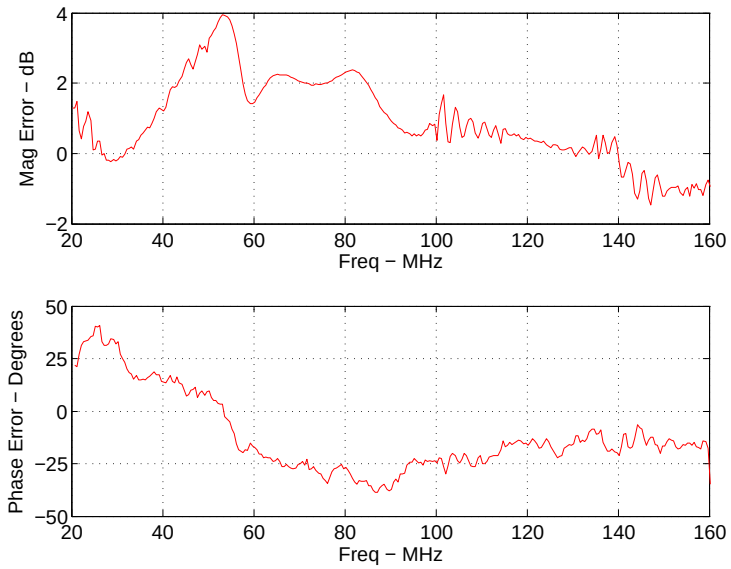


Figure 6.30: S_{21} Error of the set SBP-70+ - 1 dB atten. - ADS5521EVM with LA trigger in Bit – 20 to 160 MHz

In the last results the phase of each tones was computed using the first and the second Nyquist band, i.e. when the wanted tone was within an odd Nyquist zone the first Nyquist zone was used to get the corresponding FFT coefficient, when the wanted tone was within an even Nyquist zone the second zone was used. This leads to the linear phase response observed on the figure 6.28.

This time, instead of the previous procedure, only the first Nyquist zone was considered. So, no matters in which Nyquist zone the tone was, the first zone was always used to get the FFT coefficient value. With this procedure, it was possible to see what happens to the phase if only a real signal has been considering. The results can be depicted on figure 6.31.

As expected from zone to zone the phase delay switches direction.

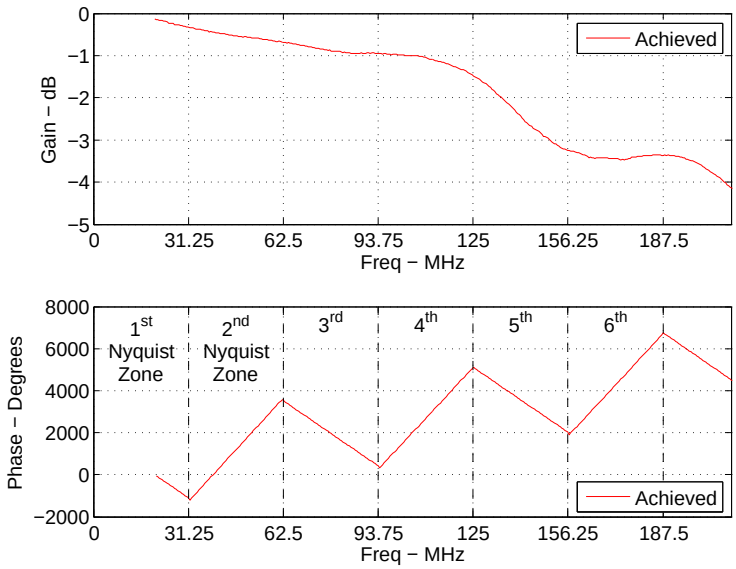


Figure 6.31: S_{21} of ADS5521EVM, measure at only the first Nyquist zone – 20 to 210 MHz

Chapter 7

Conclusion

In this dissertation the analog stage of the proposed analyzer was implemented, tested and is fully functional. The digital stage, due to problems and limitations was implemented using an Oscilloscope and a Logic Analyzer.

The analog S_{11} results are already very accurate in relation to measurements performed on a commercial VNA. Only the S_{11} phase results remains with an error around 40° at 1 GHz, whose source is still unknown.

To perform gain measurements with the suggested architecture, it was also suggested and implemented a different measurement technique. With the 2-tone technique, it was possible to deal with the limitations of the mixed-domain measurements. It is indeed a valid procedure to overcome the LO phase influence when performing measurements in instruments with a super-heterodyne front-end, as the actual VNAs. Which means, it is able to easily characterize an entire receiver (all analogue or mixed-domain), apart from its configuration (with or without down-conversion stages). So, besides its use to create a new instrument to measure mixed-mode components, it also offers the possibility to be incorporated in now-a-days instruments. An extension to actual VNAs could effectively be created.

Although, the 2-tones technique has many advantages, it has many limitation too. In first place, it only could operate in very strict conditions, i.e. the DUT has to be operated in its linear region. Further, as could be seen on the results presented, the phase errors suffer from a propagation effect to the next sweep steps. Lastly, a complete calibration could not be done due to the lack of vector values for error model parameters. These limitations are caused by the way the phase is read, as an relative phase measurement, which is also the strength of the technique and gives it its immunity to the LO phase. In conclusion, it is a great start point to perform mixed-mode measurements, but it certainly have to evolve to a more robust procedure.

Nevertheless, in conditions where the attenuation is less than 10 dB, analog S_{21} results under 1 dB error and only a few degrees error were achieved.

The mixed-domain S_{21} results achieved are confirmed using its measurement raw data to perform a response calibration of a known filter. Furthermore, the phase results obtained, produce a delay error inferior to 2% of the expected value. So, the certainty of the results are already in an high accurate state.

The dynamic range of the instrument is still much limited, below -20 dB the errors became to increase. The use of the oscilloscope, in the place of an ADC is the main reason for that, due to its limited number of bits, 8 Bits in this case. The oscilloscope was used at a low frequency

rate, cause it only has to digitize IF signals. Thus, to digitize signals at this frequency range an ADC with 14 or even 16 Bits could be used instead, which produces a much more high dynamic range.

Mixer measurements could also be performed with the proposed instrument, but they are not shown on results due to the lack of a solid source for comparison and because they aren't implemented yet on the graphical user interface developed.

7.1 Future Work

In this dissertation, ADCs were the only mixed-domain components that could be directly characterized with the built instrument. DACs are also a key component in the SDR architecture (in emitters) and so, they have to be characterized also, as proposed on the beginning of this document. To accomplish it, a digital port that is able to generate digital stimulus signal has to be present on the instrument, but this port is much like the pattern generator of the LA. Thus, the remain thing that is necessary is use this LA tool.

Furthermore, if it is possible to remotely control the Logic Analyzer, much quicker acquisitions could be performed. It also opens the door to effectively trade the oscilloscope by an ADC and maximize the dynamic range of the system, without sacrifice the quickness of the system.

To overcome the impossibility to remotely control the LA, as have been happening until now, the solution is to built the entire digital stage. Incorporate the ADCs and an FPGA to the project will even possibility the transfer of some calculations to the FPGA and speeds up even more the measurement procedure.

The future could pass through an integration of all the components in one single instrument. This architecture should has built-in generators to produce the needed signals and all the others necessary components. This fully integrated system allows for suppression of external triggers and certainly will improve the measurement synchronization reducing the errors.

The pursuit of improved methods to characterize mixed-domain components should also continue. In order to surpass the two-tone technique disadvantages, the most important is to search for an absolute phase measure. This could possibility the employment of full error correction techniques on the calibration process. It could also bring the develop of models to use on simulators, like the ones found today for analog components with S-Parameters. This immediate suggest a traditional one-tone technique, very-well known and very believed. This way the calibration with complete vector error correction models will be possible, as well as, accurate vector models for the DUT. Besides, it will possibility the operation of the DUT under non-linear conditions.

To achieve one-tone measurements one of the option is to directly receive the incident and the reflected signal, using direct digitization, as explained on [60]. However, in this scenario the dynamic range will continue to be too low. Because in order to use this process, the ADC employed in such instrument has to be an ADC like the one present on a state-of-the-art oscilloscope, with a low number of bits, to allow for a very high analog bandwidth.

In conclusion, the investigation must continue in order to join the benefits of the superhetherodyne configuration to the utilization of a one-tone calibration method.

To finish, another improvement that should be pursued is the creation of a mixed-domain multiport and balanced analyzer, as actually exist in analog VNAs[61]. The ability to directly

measure balanced inputs could lead to a direct characterization of the ADC performance, without the need for an input circuitry. So, new doors will be open and on-chip measurements could be performed.

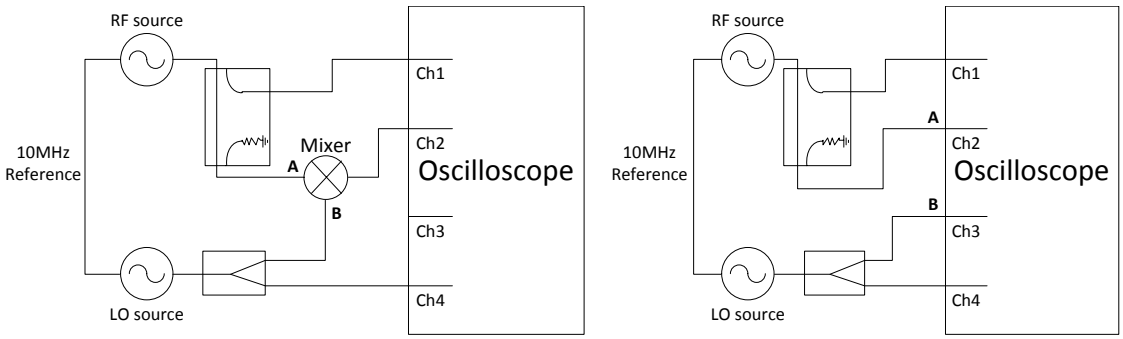
Appendix A

Translating Devices Characterization

At the IT's lab there are a lack of a VNA able to measure frequency conversion components, such as mixers. Thus, in order to characterize the mixer used to implement the instrument's analog stage and further to characterize the entire analog stage, another way to test the performance of frequency translating devices had to be searched.

The suggested solution was based on [62]. As on that the Oscilloscope will be the main instrument on the measure set. It was used the Real Time Tektronix DPO72004B, with 20 GHz bandwidth.

The lab set is depicted on figure A.1a.



(a) Measurement Lab Set

(b) Calibration Lab Set

Figure A.1: Translating Devices Measurements Lab Set

Different measures of the Mini-Circuits ZX05-5+[25] mixer were performed. The measures presented here were done with an RF signal from 20 to 1020 MHz, with an input power of -5 dBm. The LO signal used sweeps from 80 to 1080 MHz, with 14 dBm which means the mixer was fed with an 8 dBm LO. Thus, a first IF at 60 MHz(RF-LO product) will be obtained and a second at much higher frequency (RF+LO product).

In figure A.2 is shown the measured mixer conversion loss referred to each main conversion product. The results of first conversion product, at 60 MHz, are around what have been expected. From the datasheet[25] of the mixer can be seen a conversion loss around 7 dB, that are almost obtained. The results of the second conversion product began to decrease

quickly after the 700 MHz because the second IF product is near twice the RF frequency, which means after the previous frequency value, the mixer will be operated outside its work band (DC-1500 MHz).

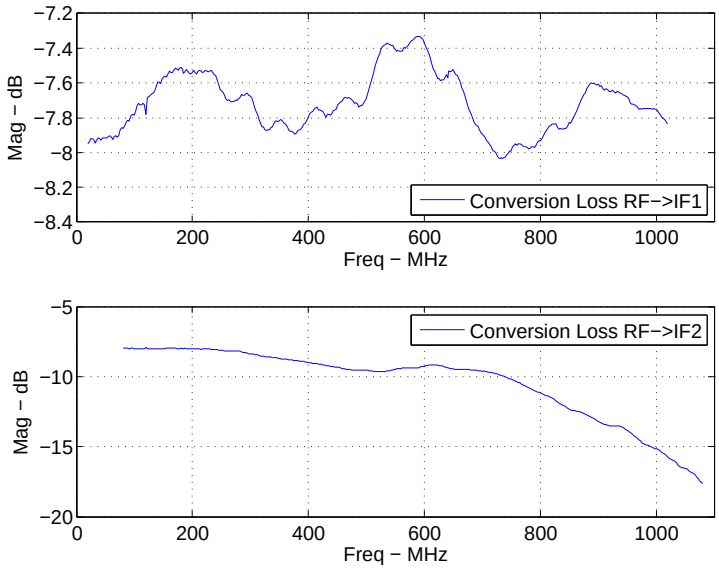


Figure A.2: Conversion Phase of the mixer ZX05-5+ – until 1100 MHz

In figure A.3 can be depicted the phase measured to each IF product. Due to the one tone nature of the measurements, absolute phase measures are accomplished.

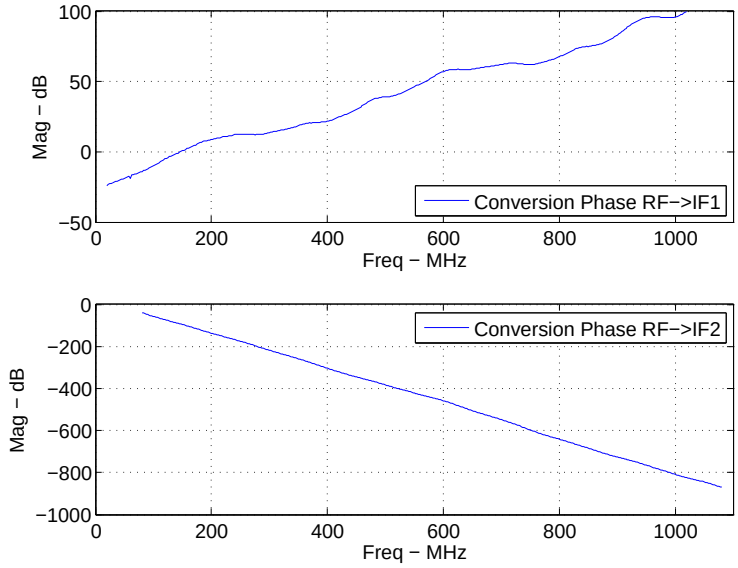


Figure A.3: Conversion Phase of the mixer ZX05-5+ – until 1100 MHz

In figure is shown the measured Isolation between the ports of the mixer.

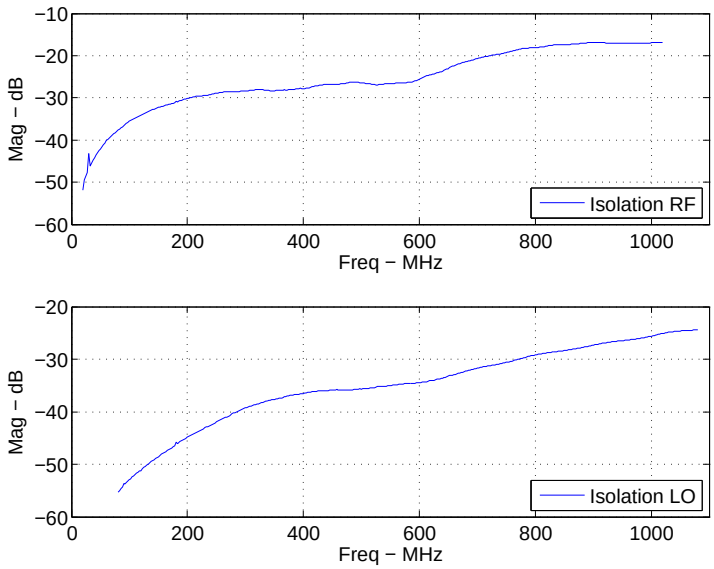


Figure A.4: Isolation between ports of the mixer ZX05-5+ – until 1100 MHz

Appendix B

GUI User's Manual

This appendix intends to describe all the functions of the Graphical User Interface (GUI) created. It will explain how a user could easily perform network measures.

The GUI is divided into 3 main windows: Main Menu, Parameters Menu and Calibration Menu.

B.1 Main Menu

When the GUI program is launched the first window that appears is shown on figure B.1. The following functions could be performed from there:

1. Goes to the Parameter Menu.
2. Goes to the Calibration Menu and displays the actual calibration state (if it is active or not).
3. Selects the type of device to characterize. The following options are available:
   - **1-Port Analog Device** – Only the analog S_{11} is measured with a 1-tone stimulus signal.
   - **2-Port Analog Device** – Both the analog S_{11} and analog S_{21} are measured with a 2-tone stimulus signal.
   - **Digital Device** – Both the analog S_{11} and digital S_{21} are measured with a 2-tone stimulus signal.
4. Proceed with measurement. During the measure the window shown on figure B.2, displays the progress of the measurement, an "`Cancel`" button is available to stop the measurement.
5. Choose to display the S_{11} or the S_{21}(when performed) measure.
6. Choose between the display formats available:
   - Magnitude in dB.
   - Magnitude in Absolute value.
   - Phase in Radians (unwrapped trace).

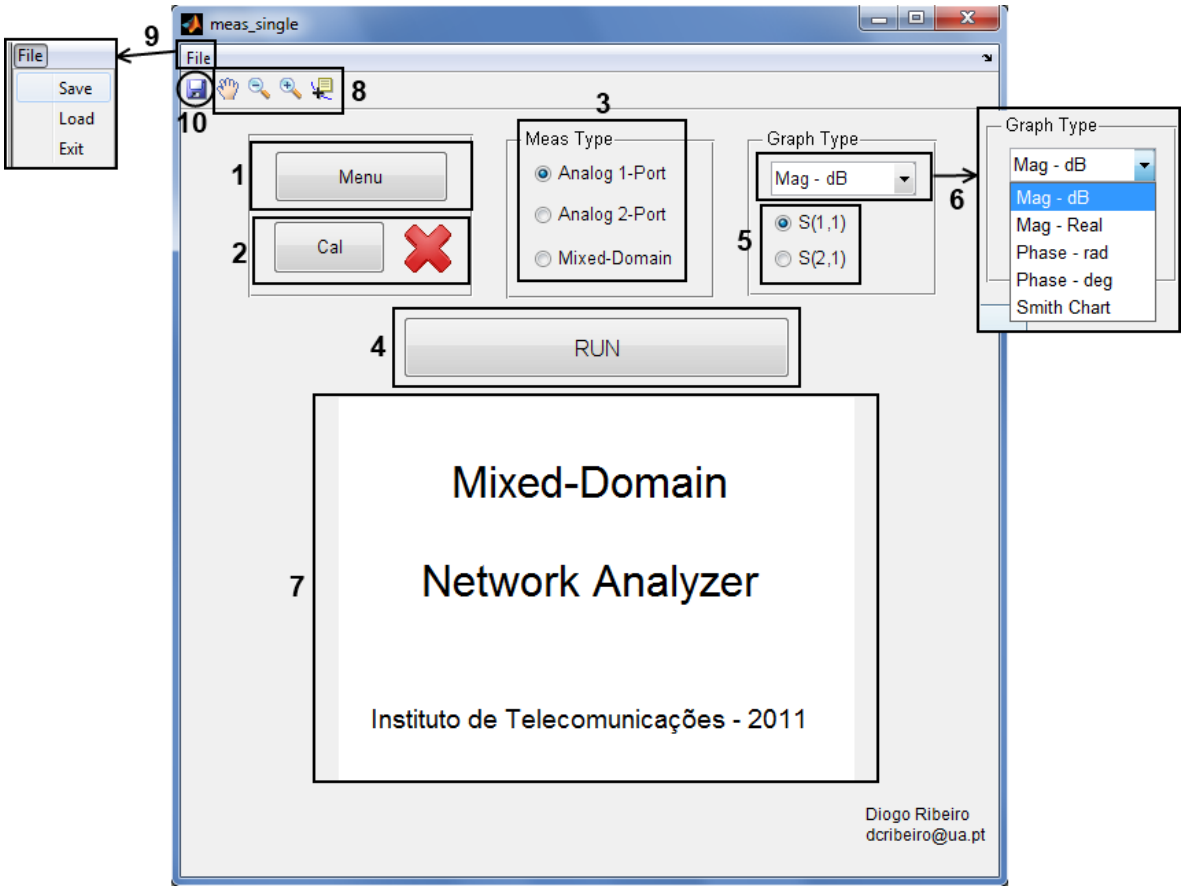


Figure B.1: GUI entry menu

- Phase in Degrees (unwrapped trace).
- Real and Complex in Smith Chart (to be available in further version).

7. Area where the result graphic will be displayed.

8. Tools to navigate on displayed graph(from MATLAB®plot tools).

9. File Menu Tab, from here it is possible to choose the following options:

   - **Save** – Save the actual calibration and results on (use the interactive menu shown on figure B.3):
     - ***.mat** file.
     - ***.s2p** file (to be implemented in further versions).
   - **Load** – Load previous calibration and results from (use an interactive menu like the one shown on figure B.3):
     - ***.mat** file.
     - ***.s2p** file (to be implemented in further versions).
   - **Exit** – Shuts down the program. The confirmation pop-up shown on figure B.4 will be displayed.

10. Save the actual calibration and results. Do the same as with **File** → **Save**.

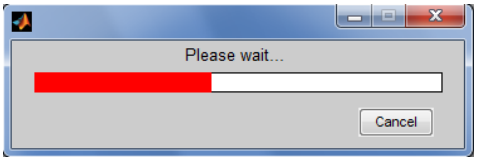


Figure B.2: GUI – Measure progress status

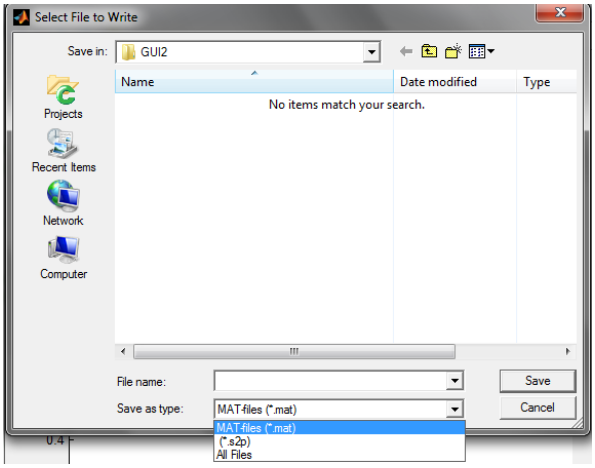


Figure B.3: GUI – Save dialogue

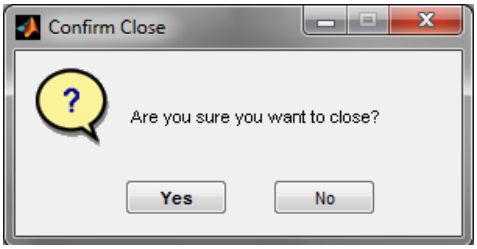


Figure B.4: GUI – Exit confirmation dialogue

B.2 Parameters Menu

In this menu the sweep parameters could be modified. In it, the following functions could be done:

1. Change the sweep Start Frequency.
2. Change the sweep Stop Frequency.
3. Change the sweep Number if Points.
4. Change the sweep type: **Linear** or **Logarithmic**(not yet implemented).
5. Change the Start and Stop Frequency units, there are available: **kHz**, **MHz** or **GHz**.
6. Change the first tone IF Frequency (in MHz).
7. Modify the Space between two consecutive frequency points (Equal to the space between tones, when valid). Influences directly the sweep Number of Points.
8. Modify the Measurement Bandwidth (The frequency resolution of the FFT).
9. Choose the Sampling frequency of the ADC to measure.
10. Choose the parameter to change when perform the parameter correction.
11. Perform the parameter Correction. Adjust the previous parameter in order to avoid measurement anomalies, described on section 5.5.
12. Adjust the power of the stimulus signal.
13. Adjust the power units of the previous parameters. The available units are: **dBW** and **dBm**.
14. Goes to the Calibration Menu
15. Goes to the Main Menu

If anyone of the parameters change, except for the stimulus power, the calibration status will be reset.

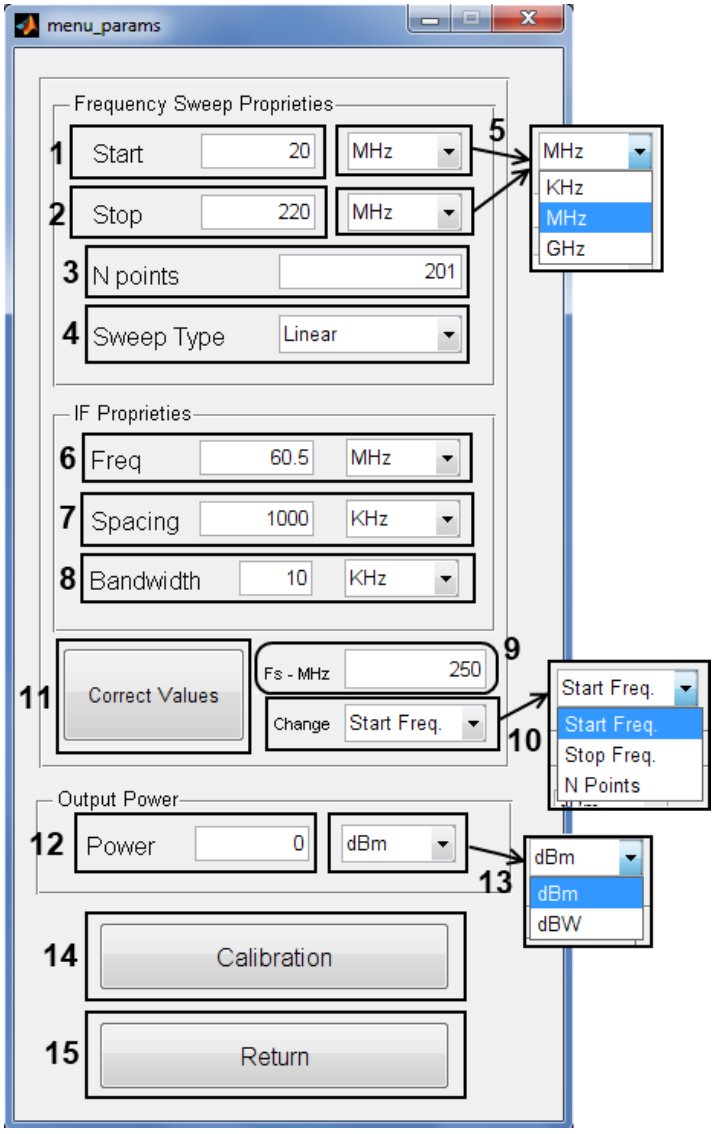


Figure B.5: GUI parameters menu

B.3 Calibration Menu

In this menu the user can perform the calibration essential to perform meaning measurements. The following options are available:

1. Perform one of the Calibration procedures:

   - **Open**
   - **Short**
   - **Load**
   - **Thru** – only allowed when it is chose the measurement of 2-Port Analog Devices, or Digital Devices.

   When any calibration button is pressed, the progress bar presented on figure B.2 is shown, in the same way it is shown when the measurement process is occurring. If the user makes a mistake and push the wrong standard button, he can push the "`Cancel`" button and everything returns to the previous state.

2. Shows the status of each calibration term. The green check mark identifies a calibration term successfully measured, while a red cross identifies a calibration term that is still not measured, for the actual parameters.

3. Saves the current calibration state and returns to the previous menu.

4. Resets all calibration terms. Each term data will be deleted and further measurements will not be affected by previous calibrations.

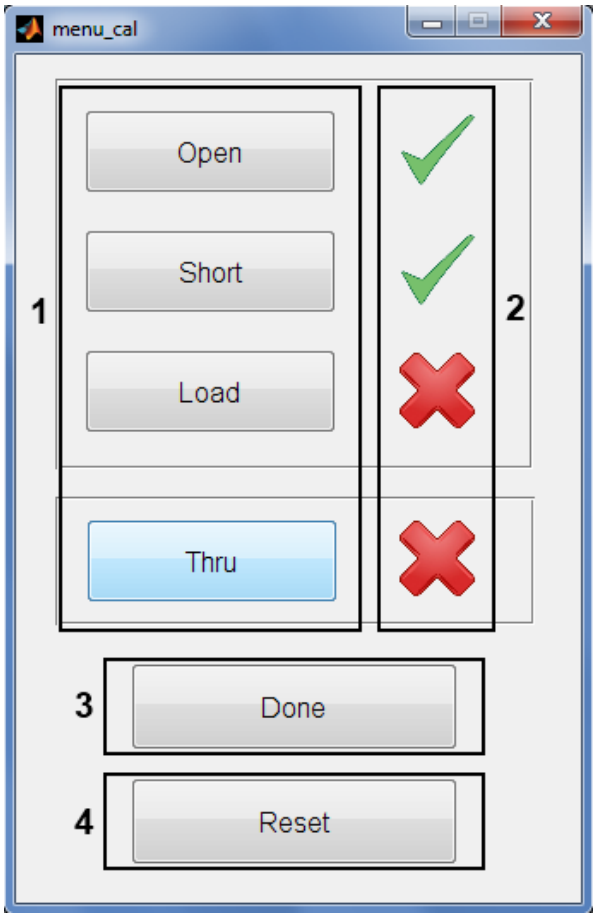


Figure B.6: GUI calibration menu

Appendix C

Boards – Schematics and PCBs

C.1 IF Filter

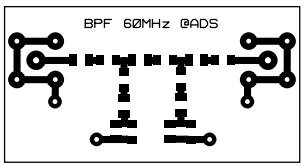


Figure C.1: BPF PCB

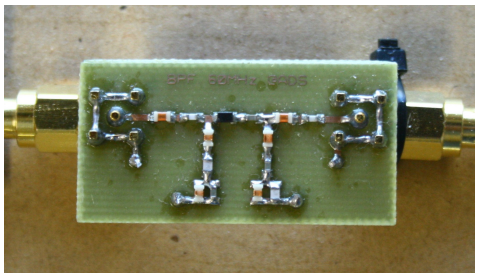


Figure C.2: BPF PCB Photo

C.2 IF Amplifier

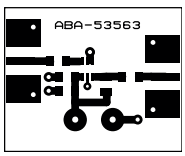


Figure C.3: ABA53563 PCB

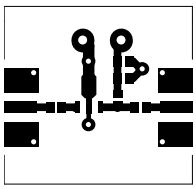


Figure C.4: ADL5536 PCB

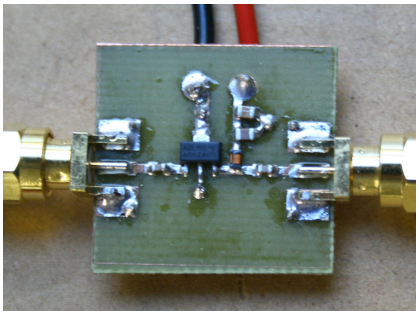


Figure C.5: ADL5536 PCB Photo

C.3 Low-Pass Filter

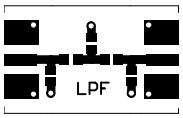


Figure C.6: LPF PCB

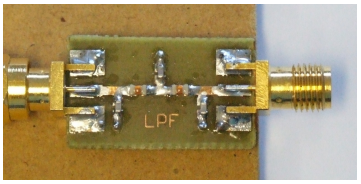


Figure C.7: LPF PCB Photo

C.4 ADC

C.4.1 Evaluation Board

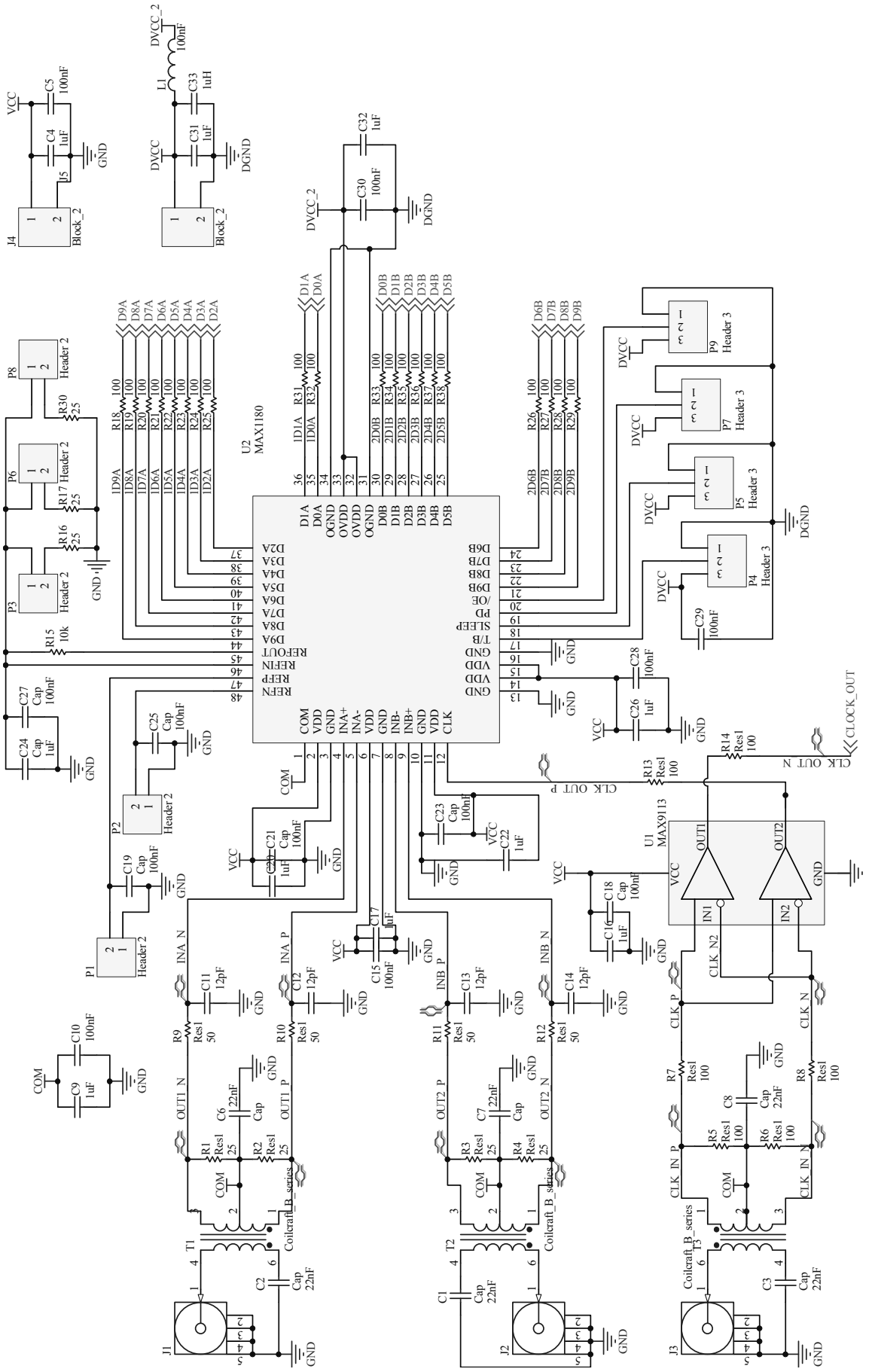


Figure C.8: ADC Schematic part 1

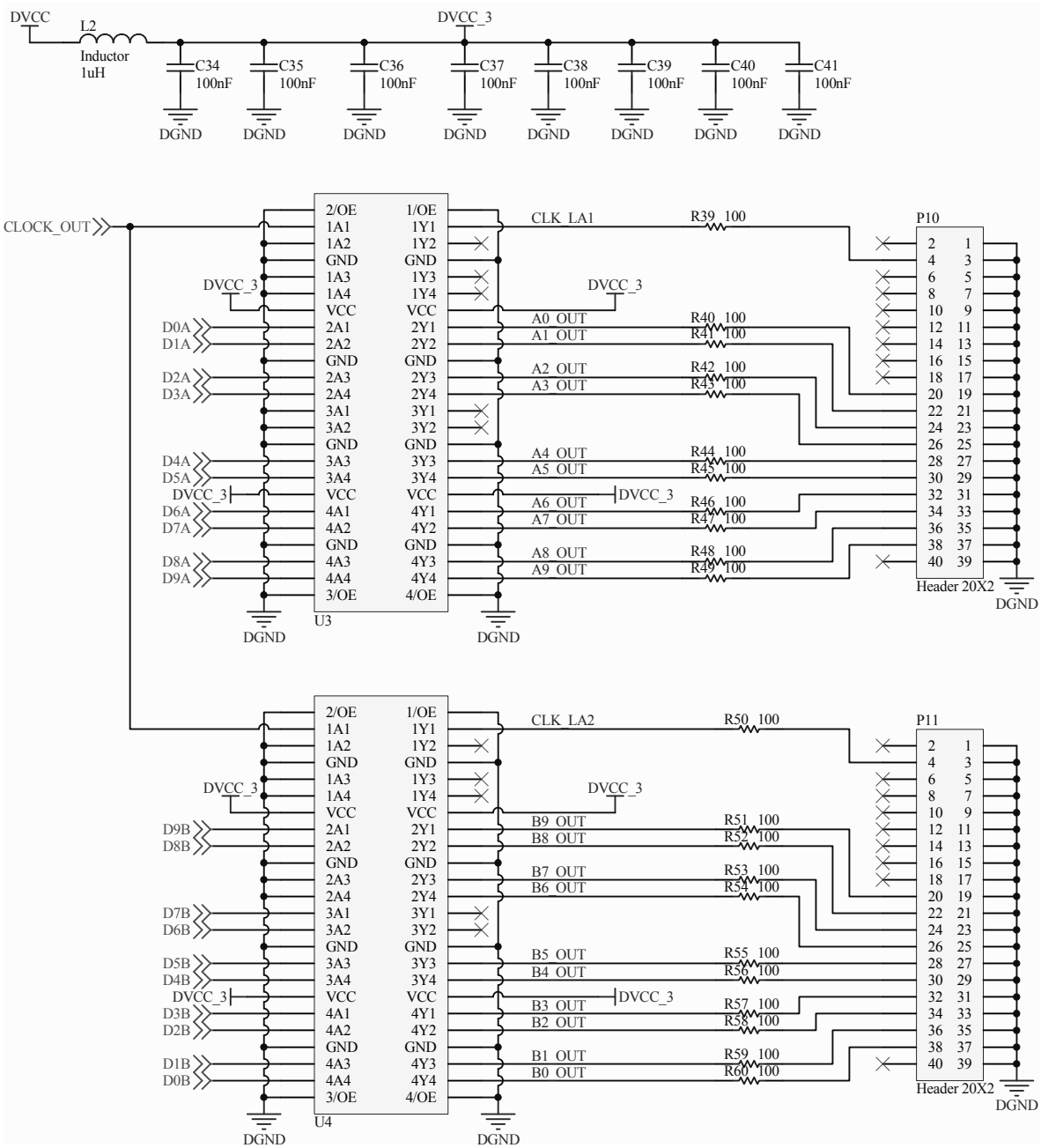


Figure C.9: ADC Schematic part 2

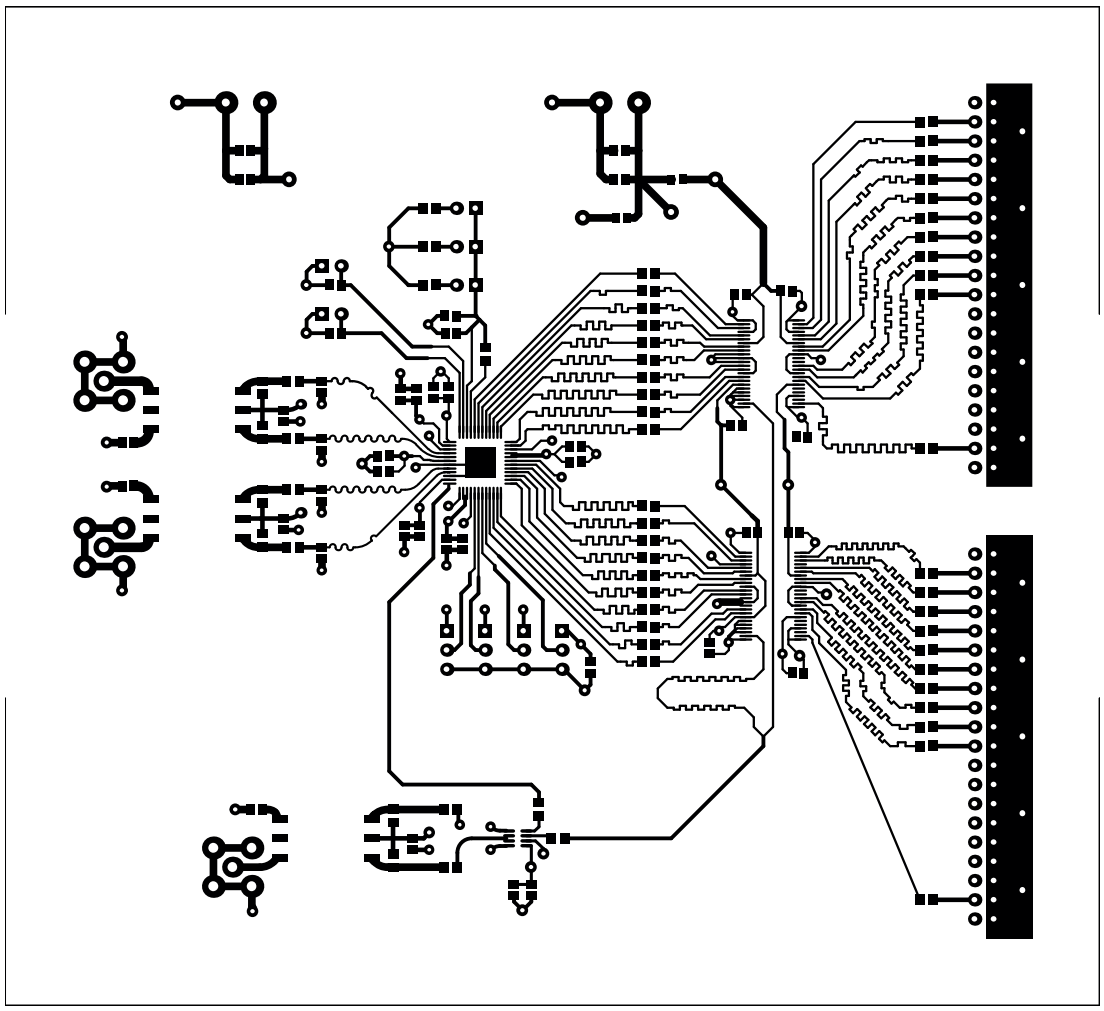


Figure C.10: ADC PCB front

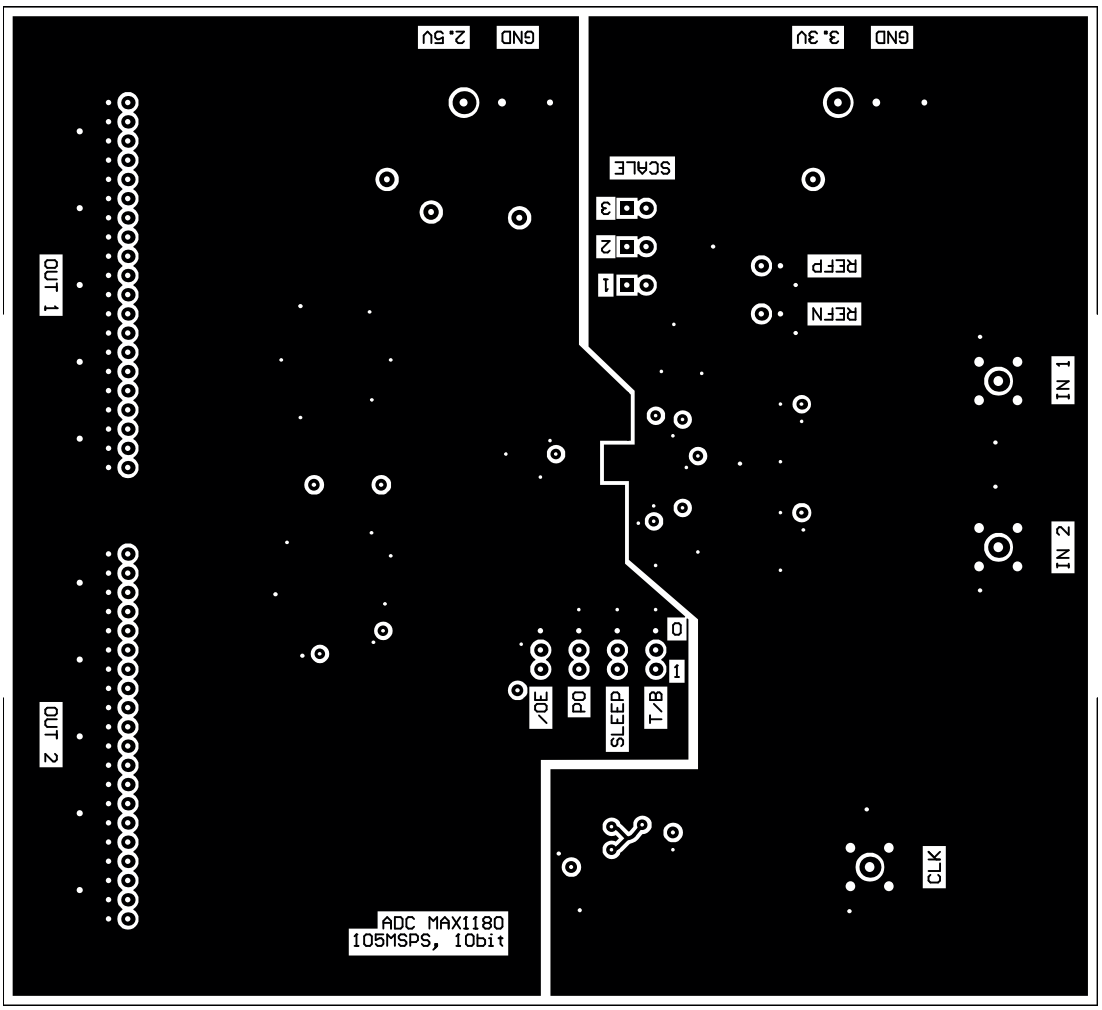


Figure C.11: ADC PCB back

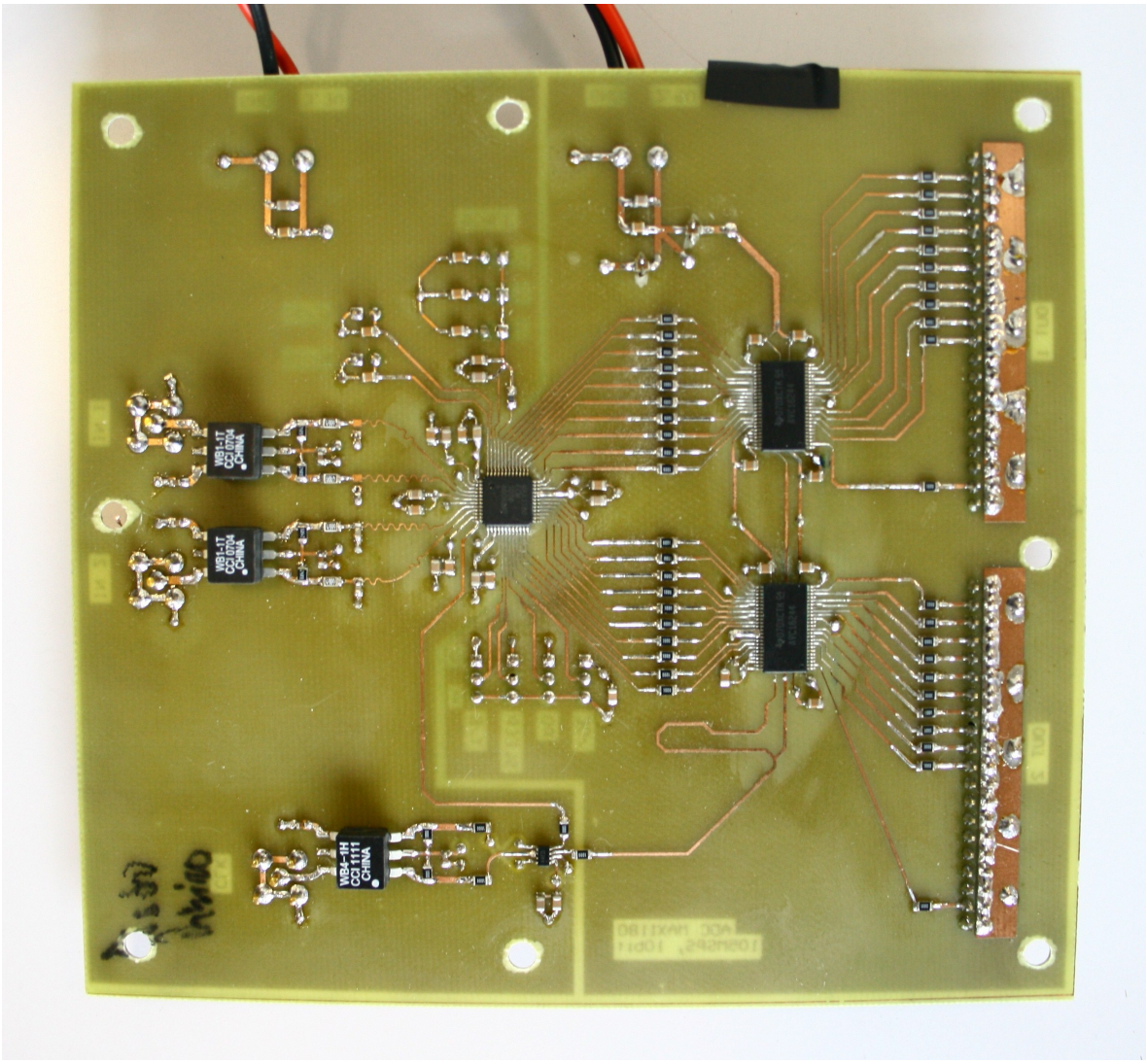


Figure C.12: ADC PCB front Photo

C.4.2 Isolation Board

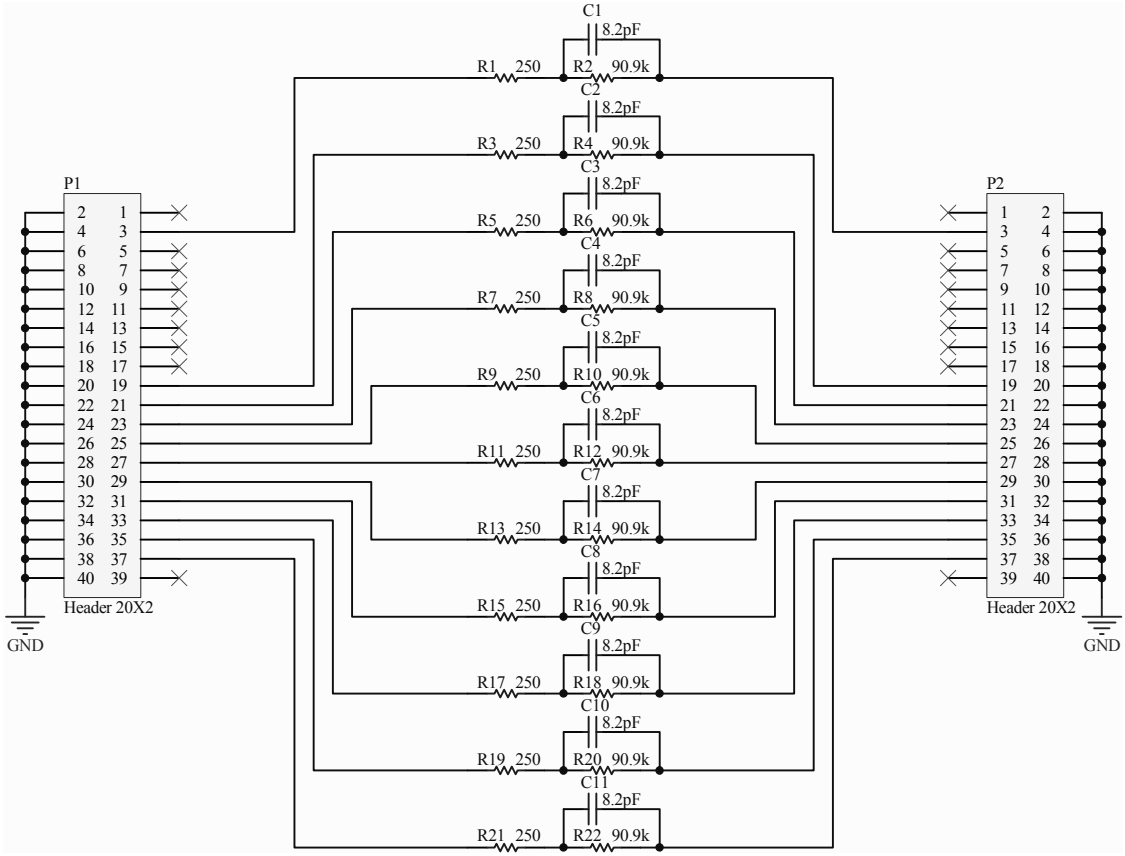


Figure C.13: ADC Isolation Schematic

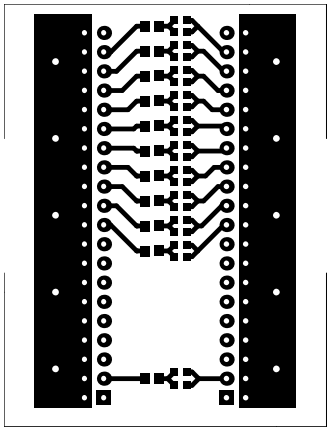


Figure C.14: ADC Isolation PCB

C.5 Power Source

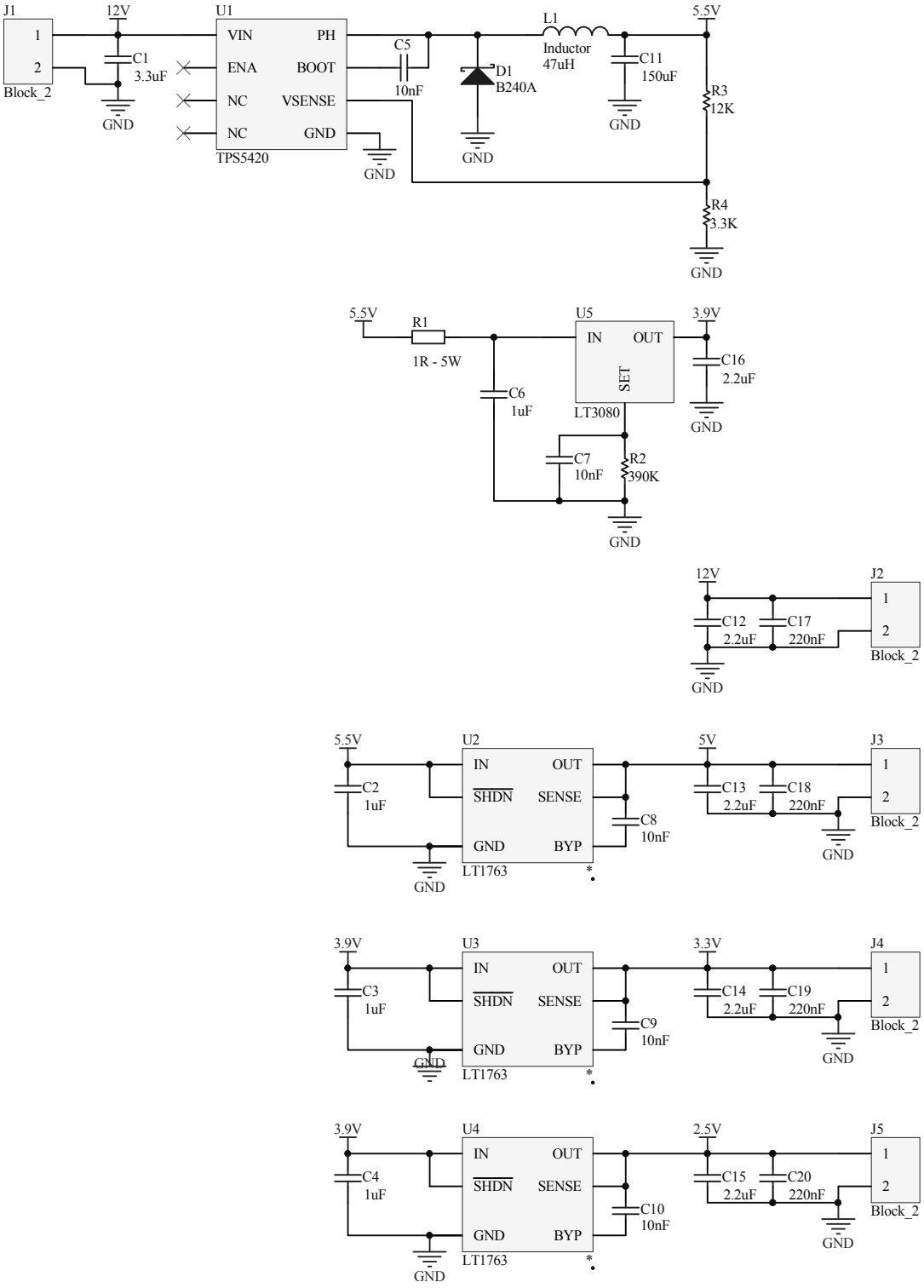


Figure C.15: Power Source Schematic

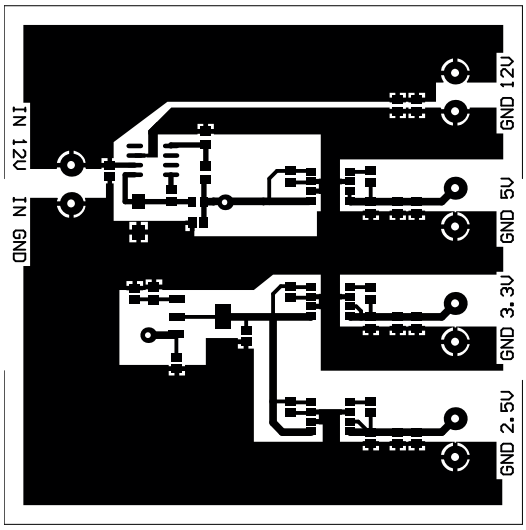


Figure C.16: Power Source PCB

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